APEX 20K

Programmable Logic Device Family

January 2001, ver. 3.3 | Data Sheet

Features...

Preliminary Information

- Industry's first programmable logic device (PLD) incorporating system-on-a-programmable-chip integration
  - MultiCore™ architecture integrating look-up table (LUT) logic, product-term logic, and embedded memory
  - LUT logic used for register-intensive functions
  - Embedded system block (ESB) used to implement memory functions, including first-in first-out (FIFO) buffers, dual-port RAM, and content-addressable memory (CAM)
  - ESB implementation of product-term logic used for combinatorial-intensive functions
- High density
  - 30,000 to 1.5 million typical gates (see Tables 1 and 2)
  - Up to 51,840 logic elements (LEs)
  - Up to 442,368 RAM bits that can be used without reducing available logic
  - Up to 3,456 product-term-based macrocells

Table 1. APEX 20K Device Features *Note (1)*

Feature	EP20K30E	EP20K60E	EP20K100	EP20K100E	EP20K160E	EP20K200	EP20K200E
Maximum system gates	113,000	162,000	263,000	263,000	404,000	526,000	526,000
Typical gates	30,000	60,000	100,000	100,000	160,000	200,000	200,000
LEs	1,200	2,560	4,160	4,160	6,400	8,320	8,320
ESBs	12	16	26	26	40	52	52
Maximum RAM bits	24,576	32,768	53,248	53,248	81,920	106,496	106,496
Maximum macrocells	192	256	416	416	640	832	832
Maximum user I/O pins	128	196	252	246	316	382	376

Table 2. APEX 20K Device Features *Note (1)*

Feature	EP20K300E	EP20K400	EP20K400E	EP20K600E	EP20K1000E	EP20K1500E
Maximum system gates	728,000	1,052,000	1,052,000	1,537,000	1,772,000	2,392,000
Typical gates	300,000	400,000	400,000	600,000	1,000,000	1,500,000
LEs	11,520	16,640	16,640	24,320	38,400	51,840
ESBs	72	104	104	152	160	216
Maximum RAM bits	147,456	212,992	212,992	311,296	327,680	442,368
Maximum macrocells	1,152	1,664	1,664	2,432	2,560	3,456
Maximum user I/O pins	408	502	488	588	708	808

Note to tables:

(1) The embedded IEEE Std. 1149.1 Joint Test Action Group (JTAG) boundary-scan circuitry contributes up to 57,000 additional gates.

...and More Features

- Designed for low-power operation
  - 1.8-V and 2.5-V supply voltage (see Table 3)
  - MultiVolt™ I/O interface support to interface with 1.8-V, 2.5-V, 3.3-V, and 5.0-V devices (see Table 3)
  - ESB offering programmable power-saving mode
- Flexible clock management circuitry with up to four phase-locked loops (PLLs)
  - Built-in low-skew clock tree
  - Up to eight global clock signals
  - ClockLock™ feature reducing clock delay and skew
  - ClockBoost™ feature providing clock multiplication and division
  - ClockShift™ programmable clock phase and delay shifting
- Powerful I/O features
  - Compliant with peripheral component interconnect Special Interest Group (PCI SIG) ***PCI Local Bus Specification, Revision 2.2*** for 3.3-V operation at 33 or 66 MHz and 32 or 64 bits
  - Support for high-speed external memories, including DDR SDRAM and ZBT SRAM (ZBT is a trademark of Integrated Device Technology, Inc.)
  - Bidirectional I/O performance (t_{CO} + t_{SU}) up to 250 MHz
  - LVDS performance up to 840 Mbits per channel
  - Direct connection from I/O pins to local interconnect providing fast t_{CO} and t_{SU} times for complex logic
  - MultiVolt I/O interface support to interface with 1.8-V, 2.5-V, 3.3-V, and 5.0-V devices (see Table 3)
  - Programmable clamp to V_{CCIO}
  - Individual tri-state output enable control for each pin
  - Programmable output slew-rate control to reduce switching noise
  - Support for advanced I/O standards, including low-voltage differential signaling (LVDS), LVPECL, PCI-X, AGP, CTT, stub-series terminated logic (SSTL-3 and SSTL-2), Gunning transceiver logic plus (GTL+), and high-speed terminated logic (HSTL Class I)
  - Supports hot-socketing operation
  - Pull-up on I/O pins before and during configuration

Table 3. APEX 20K Supply Voltages

Feature	EP20K100 EP20K200 EP20K400	EP20K30E EP20K60E EP20K100E EP20K160E EP20K200E EP20K300E EP20K400E EP20K600E EP20K1000E EP20K1500E
Internal supply voltage (V_{CCINT})	2.5 V	1.8 V
MultiVolt I/O interface voltage levels (V_{CCIO})	2.5 V, 3.3 V, 5.0 V *(1)*	1.8 V, 2.5 V, 3.3 V, 5.0 V *(2)*

Notes :
(1) Certain APEX 20K devices are 5.0-V tolerant. See "MultiVolt I/O Interface" on page 46 for details.
(2) APEX 20KE devices can be 5.0-V tolerant by using an external resistor.

- Advanced interconnect structure
  - Four-level hierarchical FastTrack® Interconnect structure providing fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Interleaved local interconnect allows one LE to drive 29 other LEs through the fast local interconnect
- Advanced packaging options
  - Available in a variety of packages with 144 to 1,020 pins (see Tables 4 through 7)
  - FineLine BGA™ packages maximize board space efficiency
- Advanced software support
  - Software design support and automatic place-and-route provided by the Altera® Quartus™ development system for Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations
  - Altera MegaCore® functions and Altera Megafunction Partners Program (AMPP℠) megafunctions
  - NativeLink™ integration with popular synthesis, simulation, and timing analysis tools

- Quartus SignalTap™ embedded logic analyzer simplifies in-system design evaluation by giving access to internal nodes during device operation
- Supports popular revision-control software packages including PVCS, Revision Control System(RCS), and Source Code Control System(SCCS)

Table 4. APEX 20K QFP, BGA & PGA Package Options & I/O Count *Notes (1), (2)*

Device	144-Pin TQFP	208-Pin PQFP RQFP	240-Pin PQFP RQFP	356-Pin BGA	652-Pin BGA	655-Pin PGA
EP20K30E	92	125				
EP20K60E	92	148	151	196		
EP20K100	101	159	189	252		
EP20K100E	92	151	183	246		
EP20K160E	88	143	175	271		
EP20K200		144	174	277		
EP20K200E		136	168	271	376	
EP20K300E			152		408	
EP20K400					502	502
EP20K400E					488	
EP20K600E					488	
EP20K1000E					488	
EP20K1500E					488	

Table 5. APEX 20K FineLine BGA Package Options & I/O Count *, Notes (1), (2)*

Device	144-Pin	324-Pin	484-Pin	672-Pin	1,020-Pin
EP20K30E	93	128			
EP20K60E	93	196			
EP20K100		252			
EP20K100E	93	246			
EP20K160E			316		
EP20K200			382		
EP20K200E			376	376	
EP20K300E				408	
EP20K400				502 *(3)*	
EP20K400E				488 *(3)*	
EP20K600E				508 *(3)*	588
EP20K1000E				508 *(3)*	708
EP20K1500E					808

Notes to tables:
(1) I/O counts include dedicated input and clock pins.
(2) APEX 20K device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), 1.27-mm pitch ball-grid array (BGA), 1.00-mm pitch FineLine BGA, and pin-grid array (PGA) packages.
(3) This device uses a thermally enhanced package, which is taller than the regular package. Consult the Altera Device Package Information Data Sheet for detailed package size information.

Table 6. APEX 20K QFP, BGA & PGA Package Sizes

Feature	144-Pin TQFP	208-Pin QFP	240-Pin QFP	356-Pin BGA	652-Pin BGA	655-Pin PGA
Pitch (mm)	0.50	0.50	0.50	1.27	1.27	–
Area (mm^2)	484	924	1,218	1,225	2,025	3,906
Length × Width (mm × mm)	22 × 22	30.4 × 30.4	34.9 × 34.9	35 × 35	45 × 45	62.5 × 62.5

Table 7. APEX 20K FineLine BGA Package Sizes

Feature	144-Pin	324-Pin	484-Pin	672-Pin	1,020-Pin
Pitch (mm)	1.00	1.00	1.00	1.00	1.00
Area (mm^2)	169	361	529	729	1,089
Length × Width (mm × mm)	13 × 13	19 × 19	23 × 23	27 × 27	33 × 33

General Description

APEX™ 20K devices are the first PLDs designed with the MultiCore architecture, which combines the strengths of LUT-based and product-term-based devices with an enhanced memory structure. LUT-based logic provides optimized performance and efficiency for data-path, register-intensive, mathematical, or digital signal processing (DSP) designs. Product-term-based logic is optimized for complex combinatorial paths, such as complex state machines. LUT- and product-term-based logic combined with memory functions and a wide variety of MegaCore and AMPP functions make the APEX 20K architecture uniquely suited for system-on-a-programmable-chip designs. Applications historically requiring a combination of LUT-, product-term-, and memory-based devices can now be integrated into one APEX 20K device.

APEX 20KE devices are a superset of APEX 20K devices and include additional features such as advanced I/O standard support, CAM, additional global clocks, and enhanced ClockLock clock circuitry. In addition, APEX 20KE devices extend the APEX 20K family to over one million gates. APEX 20KE devices are denoted with an "E" suffix in the device name (e.g., the EP20K1000E device is an APEX 20KE device). Table 8 compares the features included in APEX 20K and APEX 20KE devices.

Table 8. Comparison of APEX 20K & APEX 20KE Features

Feature	APEX 20K Devices	APEX 20KE Devices
MultiCore system integration	Full support	Full support
Hot-socketing support	Full support	Full support
SignalTap logic analysis	Full support	Full support
32/64-Bit, 33-MHz PCI	Full compliance in -1, -2 speed grades	Full compliance in -1, -2 speed grades
32/64-Bit, 66-MHz PCI	-	Full compliance in -1 speed grade
MultiVolt I/O	2.5-V or 3.3-V V_{CCIO} V_{CCIO} selected for device Certain devices are 5.0-V tolerant	1.8-V, 2.5-V, or 3.3-V V_{CCIO} V_{CCIO} selected block-by-block 5.0-V tolerant with use of external resistor
ClockLock support	Clock delay reduction 2× and 4× clock multiplication	Clock delay reduction $m/(n \times v)$ clock multiplication Drive ClockLock output off-chip External clock feedback ClockShift LVDS support Up to four PLLs ClockShift, clock phase adjustment
Dedicated clock and input pins	Six	Eight
I/O standard support	2.5-V, 3.3-V, 5.0-V I/O 3.3-V PCI Low-voltage complementary metal-oxide semiconductor (LVCMOS) Low-voltage transistor-to-transistor logic (LVTTL)	1.8-V, 2.5-V, 3.3-V, 5.0-V I/O 2.5-V I/O 3.3-V PCI and PCI-X 3.3-V Advanced Graphics Port (AGP) Center tap terminated (CTT) GTL+ LVCMOS LVTTL True-LVDS and LVPECL data pins up to 840 Mbps (in EP20K300E and larger devices) LVDS and LVPECL clock pins (in all devices) LVDS and LVPECL data pins up to 156 Mbps (in all devices) HSTL Class I PCI-X SSTL-2 Class I and II SSTL-3 Class I and II
Memory support	Dual-port RAM FIFO RAM ROM	CAM Dual-port RAM FIFO RAM ROM

All APEX 20K devices are reconfigurable and are 100% tested prior to shipment. As a result, test vectors do not have to be generated for fault coverage purposes. Instead, the designer can focus on simulation and design verification. In addition, the designer does not need to manage inventories of different application-specific integrated circuit (ASIC) designs; APEX 20K devices can be configured on the board for the specific functionality required.

APEX 20K devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers in-system programmability (ISP)-capable EPC1 and EPC2 configuration devices, which configure APEX 20K devices via a serial data stream. Moreover, APEX 20K devices contain an optimized interface that permits microprocessors to configure APEX 20K devices serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat APEX 20K devices as memory and configure the device by writing to a virtual memory location, making reconfiguration easy.

 Contact Altera for information on future configuration devices.

After an APEX 20K device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Real-time changes can be made during system operation, enabling innovative reconfigurable computing applications.

APEX 20K devices are supported by the Altera Quartus development system, a single, integrated package that offers HDL and schematic design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, SignalTap logic analysis, and device configuration. The Quartus software runs on Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations.

The Quartus software provides NativeLink interfaces to other industry-standard PC- and UNIX workstation-based EDA tools. For example, designers can invoke the Quartus software from within third-party design tools. Further, the Quartus software contains built-in optimized synthesis libraries; synthesis tools can use these libraries to optimize designs for APEX 20K devices. For example, the Synopsys Design Compiler library, supplied with the Quartus development system, includes DesignWare functions optimized for the APEX 20K architecture.

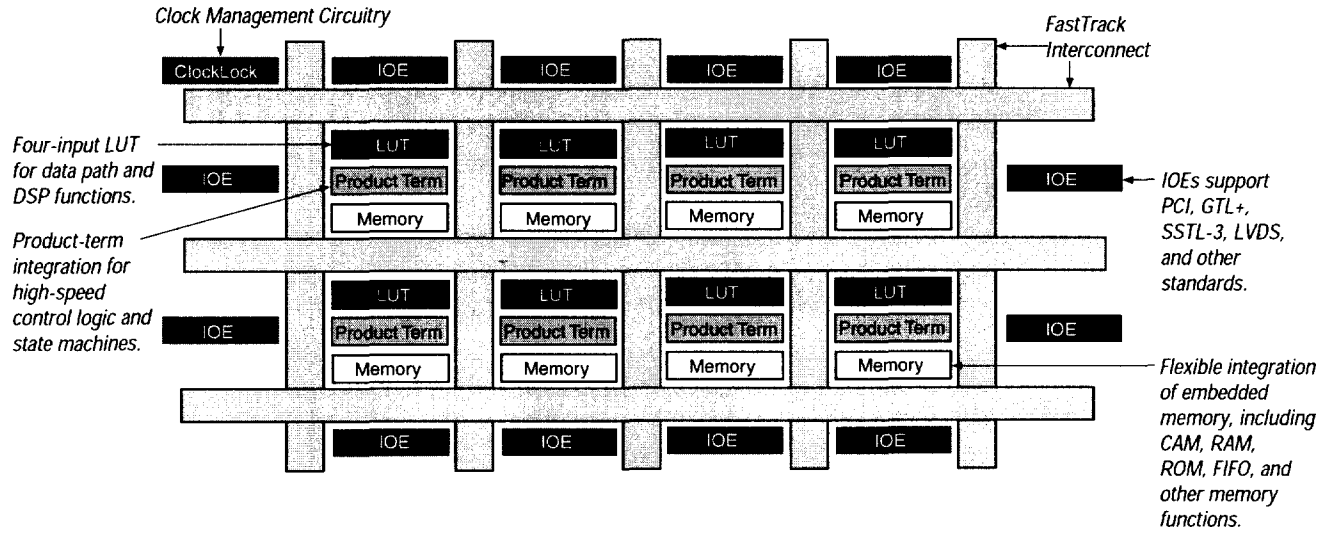
Functional Description

APEX 20K devices incorporate LUT-based logic, product-term-based logic, and memory into one device. Signal interconnections within APEX 20K devices (as well as to and from device pins) are provided by the FastTrack Interconnect—a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack Interconnect. Each IOE contains a bidirectional I/O buffer and a register that can be used as either an input or output register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. IOEs provide a variety of features, such as 3.3-V, 64-bit, 66-MHz PCI compliance; JTAG BST support; slew-rate control; and tri-state buffers. APEX 20KE devices offer enhanced I/O support, including support for 1.8-V I/O, 2.5-V I/O, LVCMOS, LVTTL, LVPECL, 3.3-V PCI, PCI-X, LVDS, GTL+, SSTL-2, SSTL-3, HSTL, CTT, and 3.3-V AGP I/O standards.

The ESB can implement a variety of memory functions, including CAM, RAM, dual-port RAM, ROM, and FIFO functions. Embedding the memory directly into the die improves performance and reduces die area compared to distributed-RAM implementations. Moreover, the abundance of cascadable ESBs ensures that the APEX 20K device can implement multiple wide memory blocks for high-density designs. The ESB's high speed ensures it can implement small memory blocks without any speed penalty. The abundance of ESBs ensures that designers can create as many different-sized memory blocks as the system requires. Figure 1 shows an overview of the APEX 20K device.

Figure 1. APEX 20K Device Block Diagram

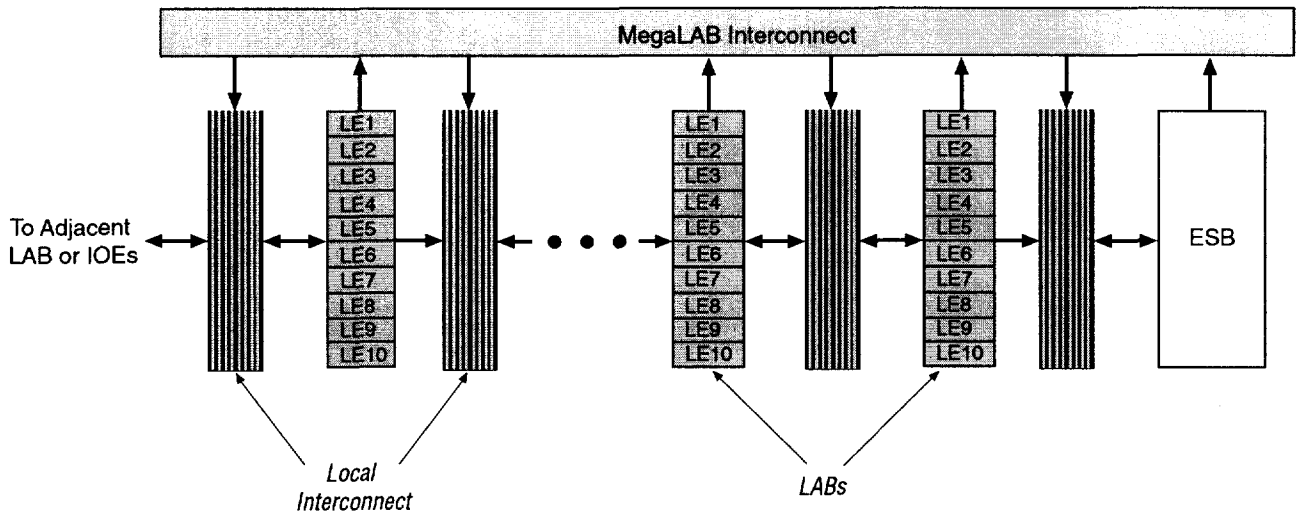


APEX 20K devices provide two dedicated clock pins and four dedicated input pins that drive register control inputs. These signals ensure efficient distribution of high-speed, low-skew control signals. These signals use dedicated routing channels to provide short delays and low skews. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or internally generated asynchronous clear signals with high fan-out. The dedicated clock pins featured on the APEX 20K devices can also feed logic. The devices also feature ClockLock and ClockBoost clock management circuitry. APEX 20KE devices provide two additional dedicated clock pins, for a total of four dedicated clock pins.

MegaLAB Structure

APEX 20K devices are constructed from a series of MegaLAB™ structures. Each MegaLAB structure contains 16 logic array blocks (LABs), one ESB, and a MegaLAB interconnect, which routes signals within the MegaLAB structure. In EP20K1000E and EP20K1500E devices, MegaLAB structures contain 24 LABs. Signals are routed between MegaLAB structures and I/O pins via the FastTrack Interconnect. In addition, edge LABs can be driven by I/O pins through the local interconnect. Figure 2 shows the MegaLAB structure.

Figure 2. MegaLAB Structure

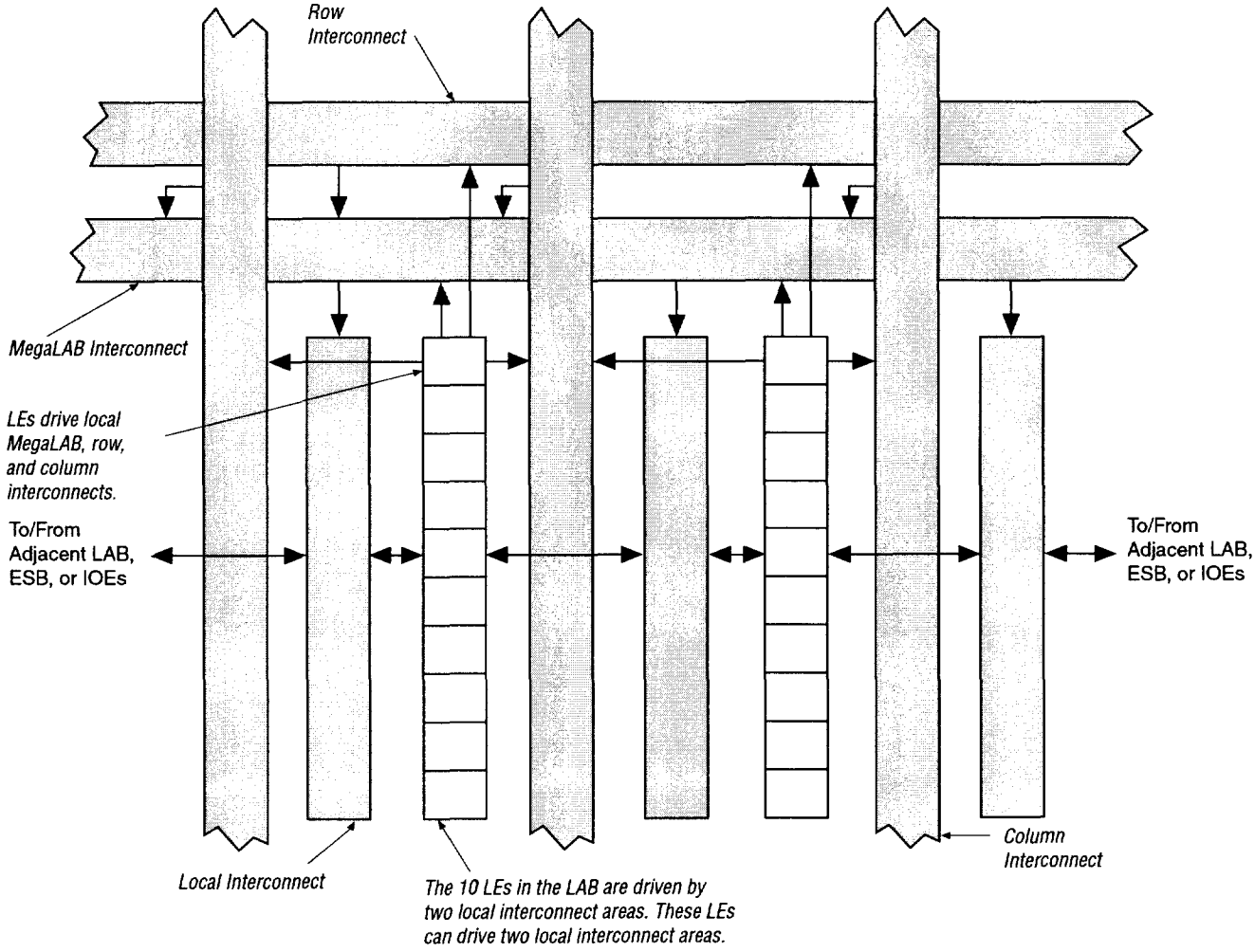


Logic Array Block

Each LAB consists of 10 LEs, the LEs' associated carry and cascade chains, LAB control signals, and the local interconnect. The local interconnect transfers signals between LEs in the same or adjacent LABs, IOEs, or ESBs. The Quartus Compiler places associated logic within an LAB or adjacent LABs, allowing the use of a fast local interconnect for high performance. Figure 3 shows the APEX 20K LAB.

APEX 20K devices use an interleaved LAB structure. This structure allows each LE to drive two local interconnect areas. This feature minimizes use of the MegaLAB and FastTrack interconnect, providing higher performance and flexibility. Each LE can drive 29 other LEs through the fast local interconnect.

Figure 3. LAB Structure



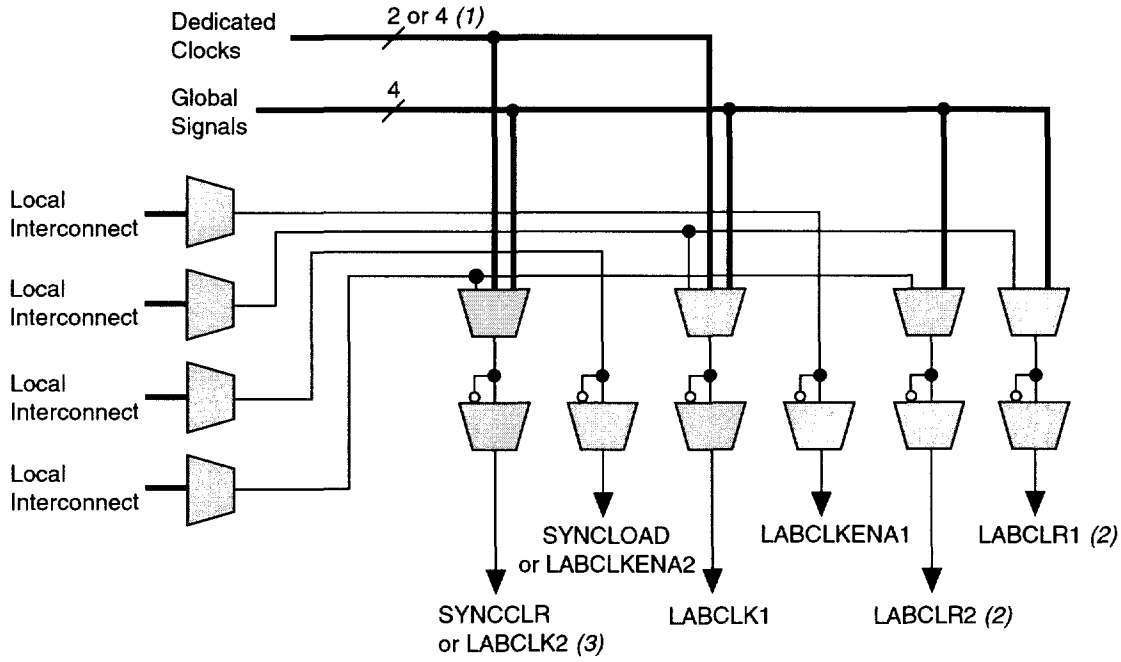
Each LAB contains dedicated logic for driving control signals to its LEs and ESBs. The control signals include clock, clock enable, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, and synchronous load signals. A maximum of six control signals can be used at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked (e.g., any LE in a particular LAB using CLK1 will also use CLKENA1). LEs with the same clock but different clock enable signals either use both clock signals in one LAB or are placed into separate LABs.

If both the rising and falling edges of a clock are used in an LAB, both LAB-wide clock signals are used.

The LAB-wide control signals can be generated from the LAB local interconnect, global signals, and dedicated clock pins. The inherent low skew of the FastTrack Interconnect enables it to be used for clock distribution. Figure 4 shows the LAB control signal generation circuit.

Figure 4. LAB Control Signal Generation

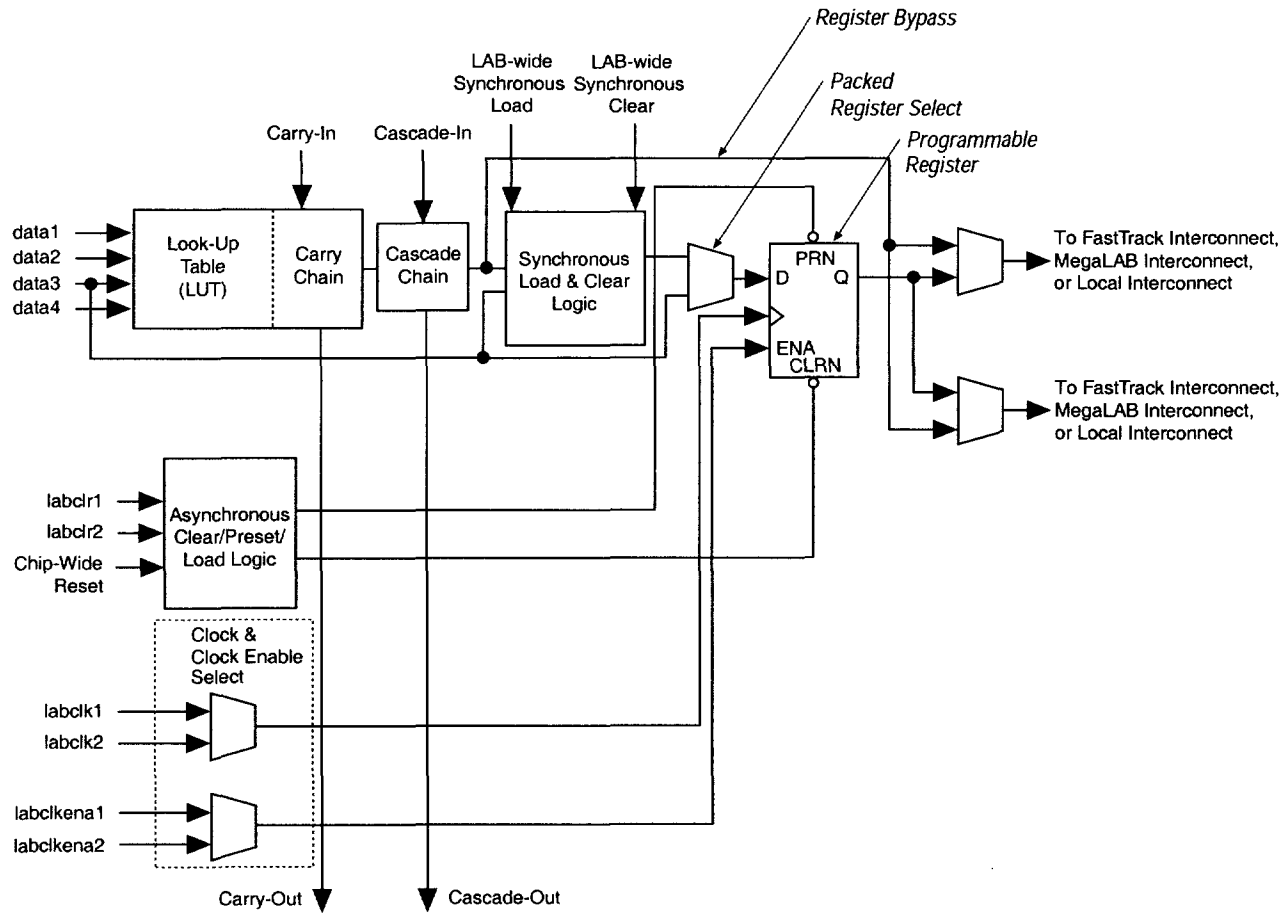


Notes:
(1) APEX 20KE devices have four dedicated clocks.
(2) The LABCLR1 and LABCLR2 signals also control asynchronous load and asynchronous preset for LEs within the LAB.
(3) The SYNCCLR signal can be generated by the local interconnect or global signals.

Logic Element

The LE, the smallest unit of logic in the APEX 20K architecture, is compact and provides efficient logic usage. Each LE contains a four-input LUT, which is a function generator that can quickly implement any function of four variables. In addition, each LE contains a programmable register and carry and cascade chains. Each LE drives the local interconnect, MegaLAB interconnect, and FastTrack Interconnect routing structures. See Figure 5.

Figure 5. APEX 20K Logic Element



Each LE's programmable register can be configured for D, T, JK, or SR operation. The register's clock and clear control signals can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the register is bypassed and the output of the LUT drives the outputs of the LE.

Each LE has two outputs that drive the local, MegaLAB, or FastTrack Interconnect routing structure. Each output can be driven independently by the LUT's or register's output. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, improves device utilization because the register and the LUT can be used for unrelated functions. The LE can also drive out registered and unregistered versions of the LUT output.

The APEX 20K architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. A carry chain supports high-speed arithmetic functions such as counters and adders, while a cascade chain implements wide-input functions such as equality comparators with minimum delay. Carry and cascade chains connect LEs 1 through 10 in an LAB and all LABs in the same MegaLAB structure.

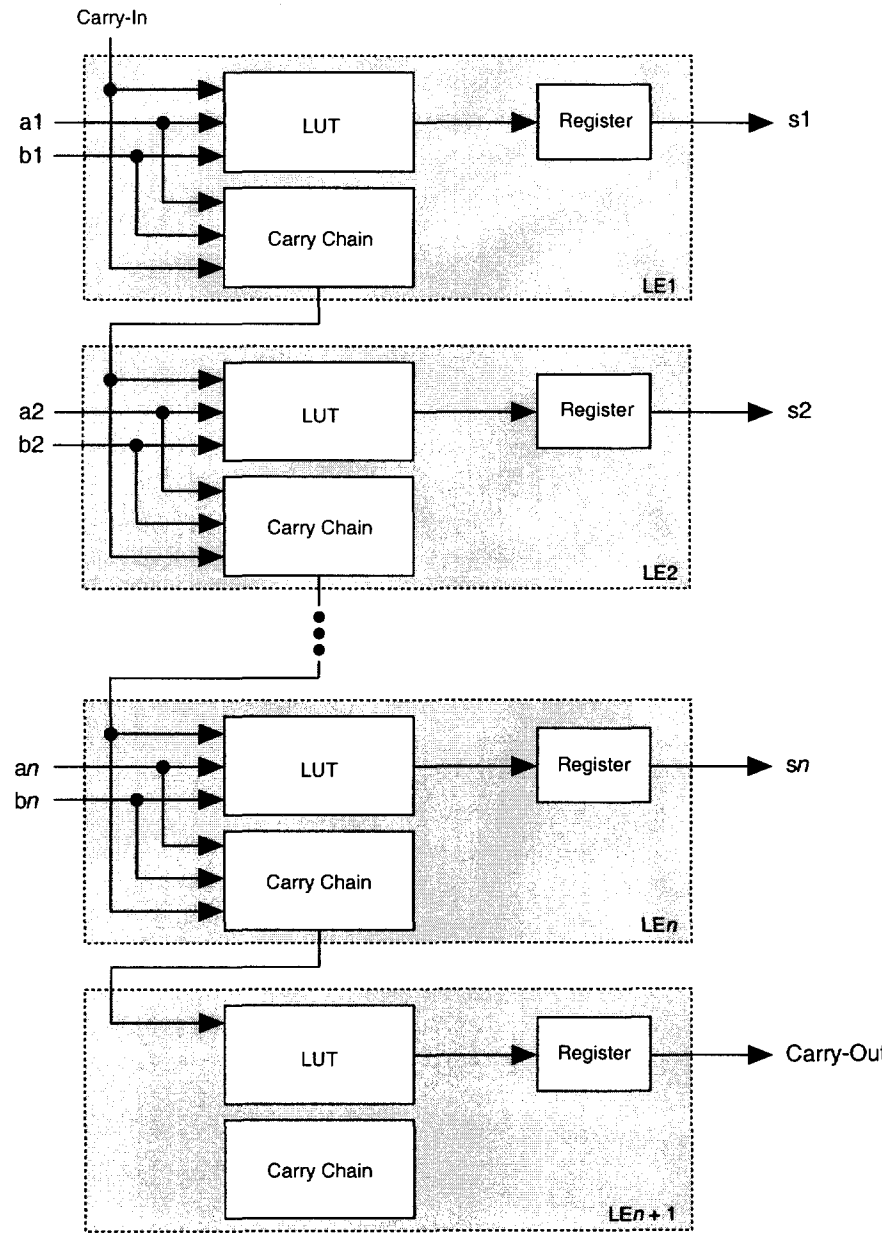
Carry Chain

The carry chain provides a very fast carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the APEX 20K architecture to implement high-speed counters, adders, and comparators of arbitrary width. Carry chain logic can be created automatically by the Quartus Compiler during design processing, or manually by the designer during design entry. Parameterized functions such as library of parameterized modules (LPM) and DesignWare functions automatically take advantage of carry chains for the appropriate functions.

The Quartus Compiler creates carry chains longer than ten LEs by linking LABs together automatically. For enhanced fitting, a long carry chain skips alternate LABs in a MegaLAB structure. A carry chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure.

Figure 6 shows how an n-bit full adder can be implemented in $n + 1$ LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the local, MegaLAB, or FastTrack Interconnect routing structures.

Figure 6. APEX 20K Carry Chain

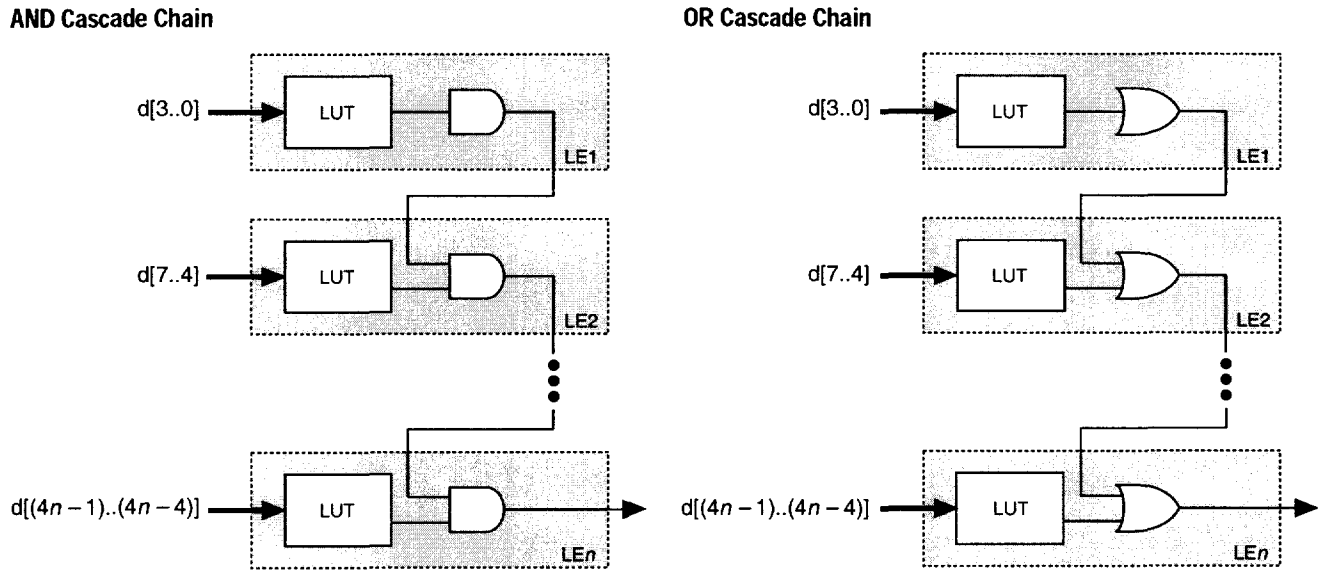


Cascade Chain

With the cascade chain, the APEX 20K architecture can implement functions with a very wide fan-in. Adjacent LUTs can compute portions of a function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a short cascade delay. Cascade chain logic can be created automatically by the Quartus Compiler during design processing, or manually by the designer during design entry.

Cascade chains longer than ten LEs are implemented automatically by linking LABs together. For enhanced fitting, a long cascade chain skips alternate LABs in a MegaLAB structure. A cascade chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure. Figure 7 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in.

Figure 7. APEX 20K Cascade Chain



LE Operating Modes

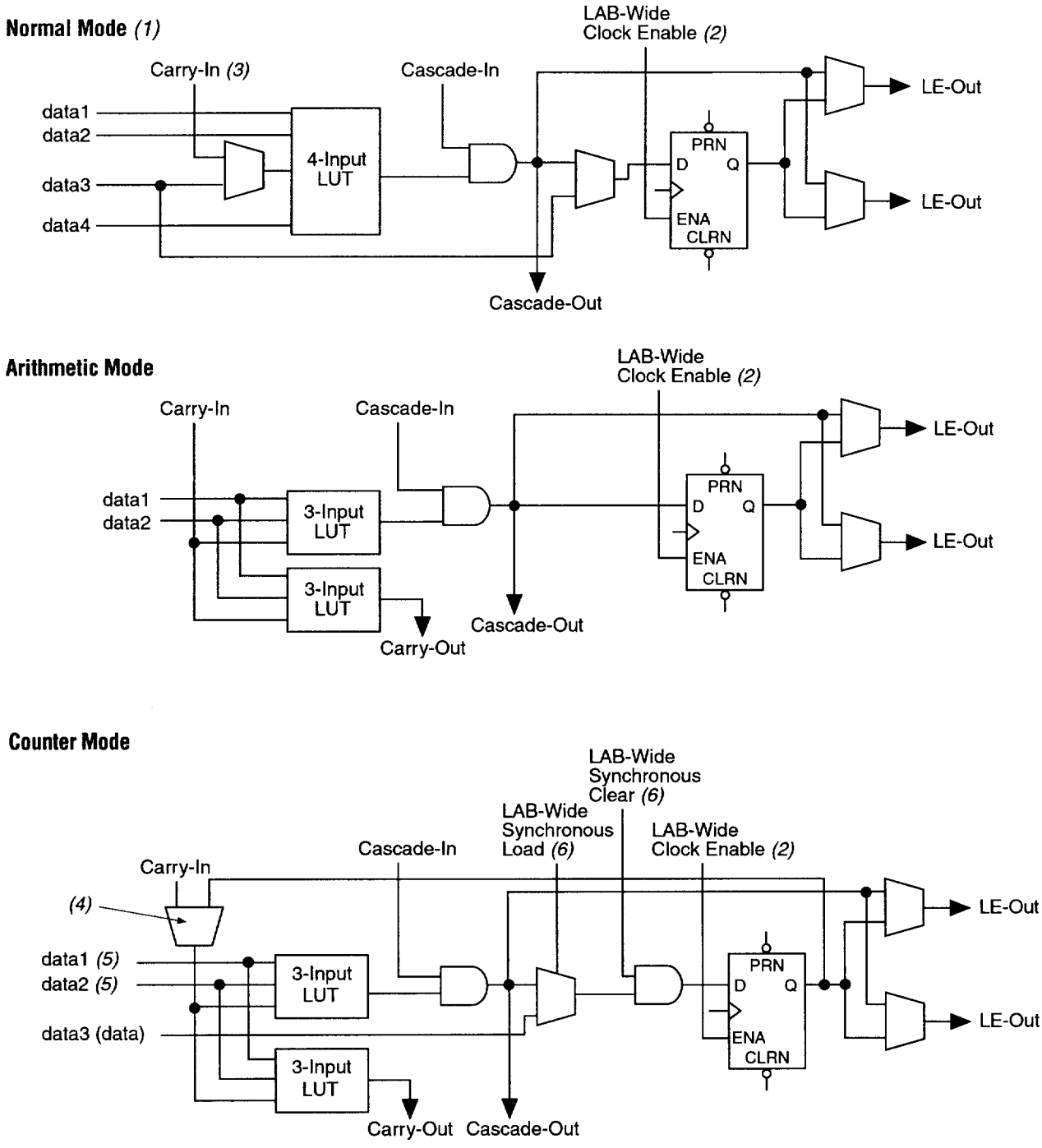
The APEX 20K LE can operate in one of the following three modes:

- Normal mode
- Arithmetic mode
- Counter mode

Each mode uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes.

The Quartus software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that specify which LE operating mode to use for optimal performance. Figure 8 shows the LE operating modes.

Figure 8. APEX 20K LE Operating Modes



Notes:

(1) LEs in normal mode support register packing.
(2) There are two LAB-wide clock enables per LAB.
(3) When using the carry-in in normal mode, the packed register feature is unavailable.
(4) A register feedback multiplexer is available on LE1 of each LAB.
(5) The DATA1 and DATA2 input signals can supply counter enable, up or down control, or register feedback signals for LEs other than the second LE in an LAB.
(6) The LAB-wide synchronous clear and LAB wide synchronous load affect all registers in an LAB.

Normal Mode

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Quartus Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. LEs in normal mode support packed registers.

Arithmetic Mode

The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a three-input function; the other generates a carry output. As shown in Figure 8, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: DATA1, DATA2, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The Quartus software implements parameterized functions that use the arithmetic mode automatically where appropriate; the designer does not need to specify how the carry chain will be used.

Counter Mode

The counter mode offers clock enable, counter enable, synchronous up/down control, synchronous clear, and synchronous load options. The counter enable and synchronous up/down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in an LAB use the counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. The Quartus software automatically places any registers that are not used by the counter into other LABs.

The counter mode uses two three-input LUTs: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading, and another AND gate provides synchronous clearing. If the cascade function is used by an LE in counter mode, the synchronous clear or load overrides any signal carried on the cascade chain. The synchronous clear overrides the synchronous load. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

Clear & Preset Logic Control

Logic for the register's clear and preset signals is controlled by LAB-wide signals. The LE directly supports an asynchronous clear function. The Quartus Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Moreover, the Quartus Compiler can use a programmable NOT-gate push-back technique to emulate simultaneous preset and clear or asynchronous load. However, this technique uses three additional LEs per register. All emulation is performed automatically when the design is compiled. Registers that emulate simultaneous preset and load will enter an unknown state upon power-up or when the chip-wide reset is asserted.

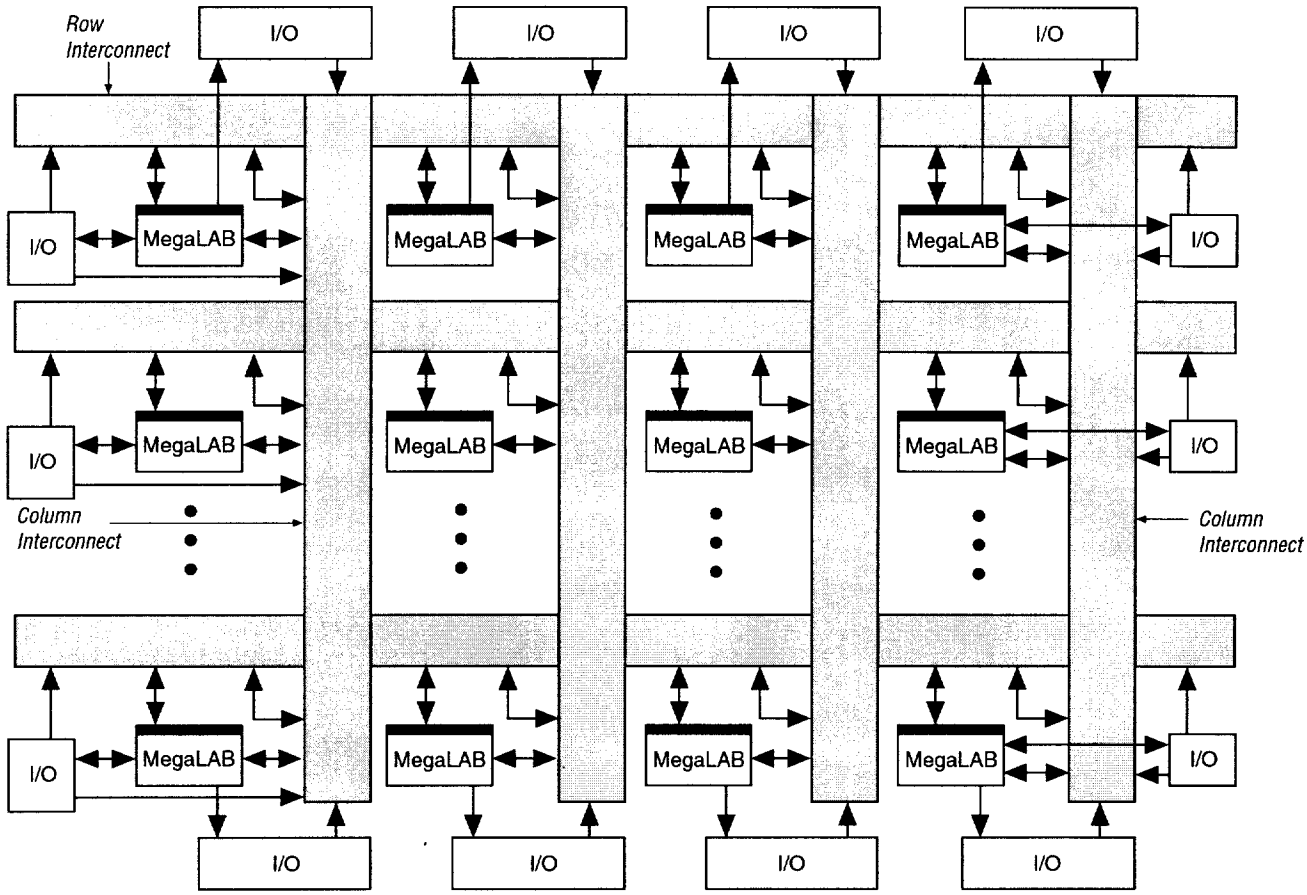
In addition to the two clear and preset modes, APEX 20K devices provide a chip-wide reset pin (DEV_CLRn) that resets all registers in the device. Use of this pin is controlled through an option in the Quartus software that is set before compilation. The chip-wide reset overrides all other control signals. Registers using an asynchronous preset are preset when the chip-wide reset is asserted; this effect results from the inversion technique used to implement the asynchronous preset.

FastTrack Interconnect

In the APEX 20K architecture, connections between LEs, ESBs, and I/O pins are provided by the FastTrack Interconnect. The FastTrack Interconnect is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack Interconnect consists of row and column interconnect channels that span the entire device. The row interconnect routes signals throughout a row of MegaLAB structures; the column interconnect routes signals throughout a column of MegaLAB structures. When using the row and column interconnect, an LE, IOE, or ESB can drive any other LE, IOE, or ESB in a device. See Figure 9.

Figure 9. APEX 20K Interconnect Structure



A row line can be driven directly by LEs, IOEs, or ESBs in that row. Further, a column line can drive a row line, allowing an LE, IOE, or ESB to drive elements in a different row via the column and row interconnect. The row interconnect drives the MegaLAB interconnect to drive LEs, IOEs, or ESBs in a particular MegaLAB structure.

A column line can be directly driven by LEs, IOEs, or ESBs in that column. A column line on a device's left or right edge can also be driven by row IOEs. The column line is used to route signals from one row to another. A column line can drive a row line; it can also drive the MegaLAB interconnect directly, allowing faster connections between rows.

Figure 10 shows how the FastTrack Interconnect uses the local interconnect to drive LEs within MegaLAB structures.

Figure 10. FastTrack Connection to Local Interconnect

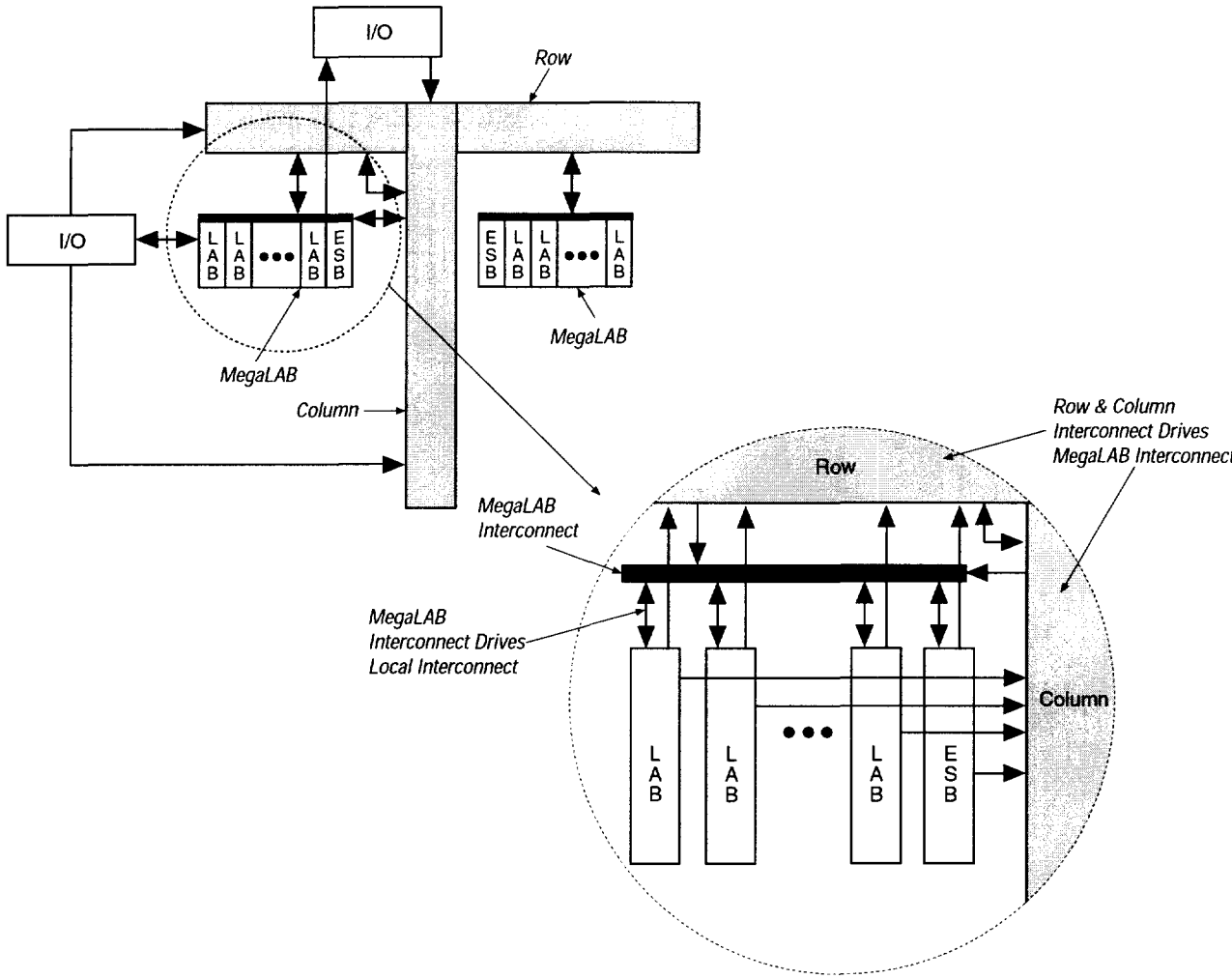
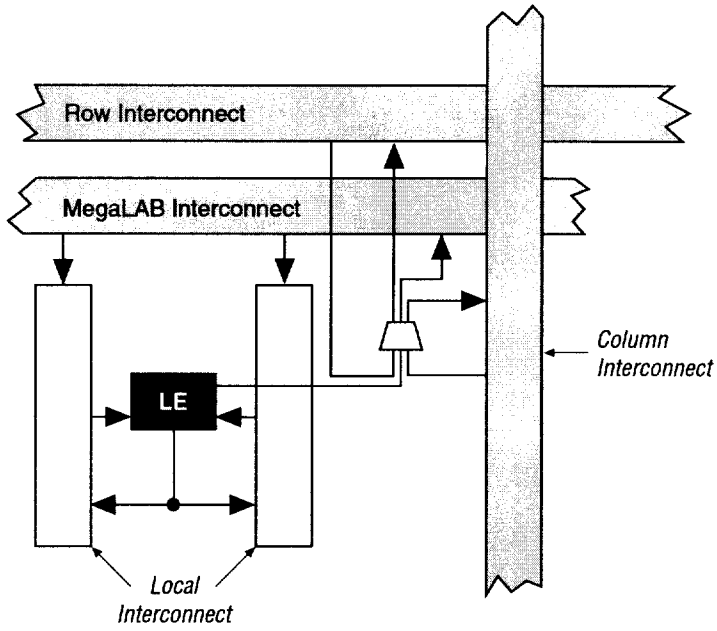


Figure 11 shows the intersection of a row and column interconnect, and how these forms of interconnects and LEs drive each other.

Figure 11. Driving the FastTrack Interconnect



APEX 20KE devices include an enhanced interconnect structure for faster routing of input signals with high fan-out. Column I/O pins can drive the FastRow interconnect, which routes signals directly into the local interconnect without having to drive through the MegaLAB interconnect. FastRow lines traverse two MegaLAB structures. Also, these pins can drive the local interconnect directly for fast setup times. On EP20K300E and larger devices, the FastRow interconnect drives the two MegaLABs in the top left corner and the two MegaLABs in the bottom right corner. On EP20K200E and smaller devices, FastRow interconnect drives the two MegaLABs on the top and the two MegaLABs on the bottom of the device. On all devices, the FastRow interconnect drives all local interconnect in the appropriate MegaLABs except the interconnect areas on the far left and far right of the MegaLAB. Pins using the FastRow interconnect achieve a faster set-up time, as the signal does not need to use a MegaLab interconnect line to reach the destination LE. Figure 12 shows the FastRow interconnect.

Figure 12. APEX 20KE FastRow Interconnect

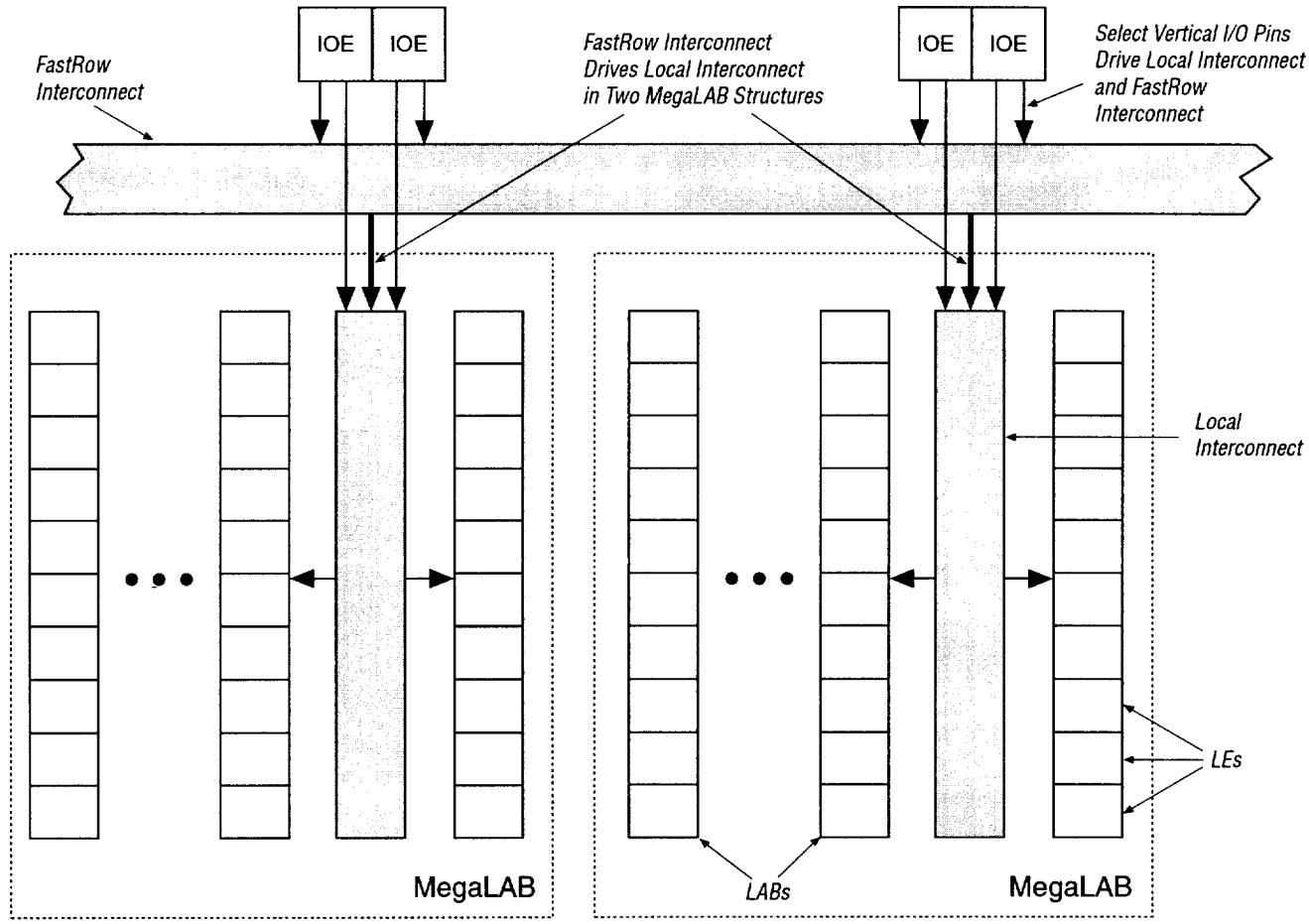


Table 9 summarizes how various elements of the APEX 20K architecture drive each other.

Table 9. APEX 20K Routing Scheme

Source	Destination								
	Row I/O Pin	Column I/O Pin	LE	ESB	Local Interconnect	MegaLAB Interconnect	Row FastTrack Interconnect	Column FastTrack Interconnect	FastRow Interconnect
Row I/O Pin					✓	✓	✓	✓	
Column I/O Pin					✓ (1)			✓	✓ (1)
LE					✓	✓	✓	✓	
ESB					✓	✓	✓	✓	
Local Interconnect	✓	✓	✓	✓					
MegaLAB Interconnect					✓				
Row FastTrack Interconnect						✓		✓	
Column FastTrack Interconnect						✓	✓		
FastRow Interconnect					✓ *(1)*				

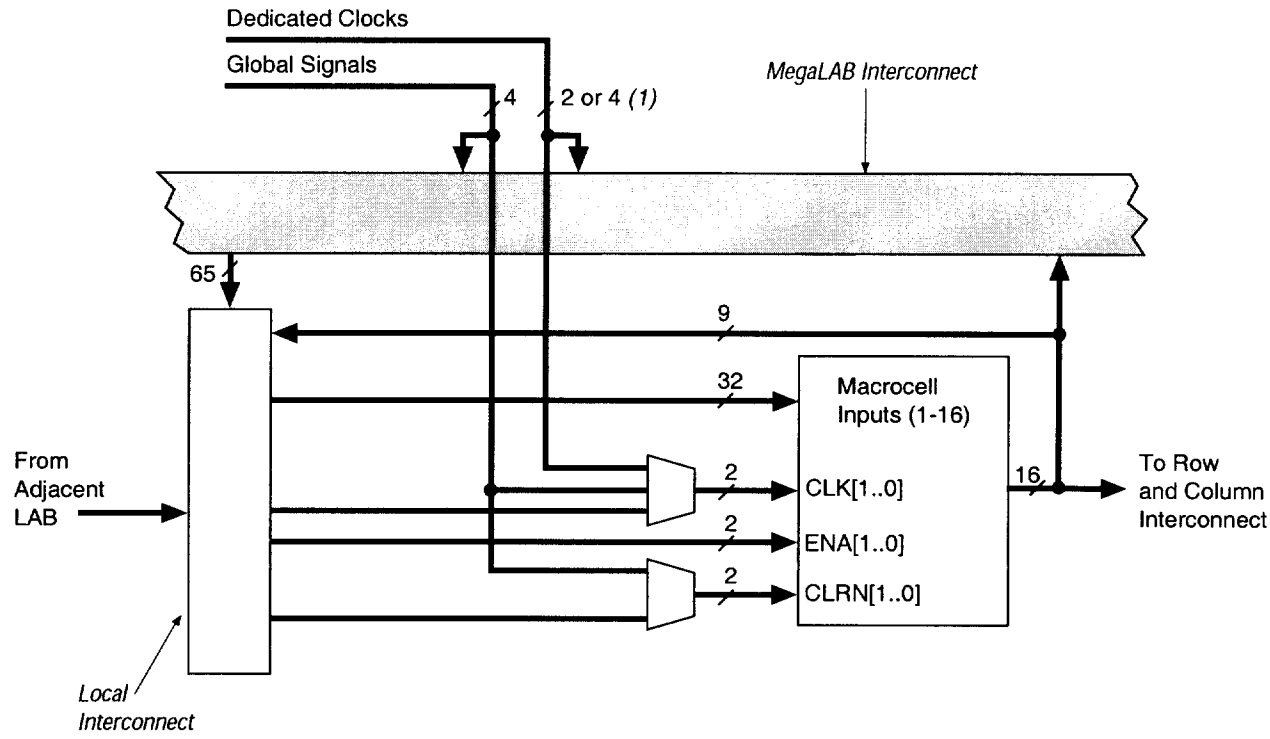
Note:
(1) This connection is supported in APEX 20KE devices only.

Product-Term Logic

The product-term portion of the MultiCore architecture is implemented with the ESB. The ESB can be configured to act as a block of macrocells on an ESB-by-ESB basis. Each ESB is fed by 32 inputs from the adjacent local interconnect; therefore, it can be driven by the MegaLAB interconnect or the adjacent LAB. Also, nine ESB macrocells feed back into the ESB through the local interconnect for higher performance. Dedicated clock pins, global signals, and additional inputs from the local interconnect drive the ESB control signals.

In product-term mode, each ESB contains 16 macrocells. Each macrocell consists of two product terms and a programmable register. Figure 13 shows the ESB in product-term mode.

Figure 13. Product-Term Logic in ESB



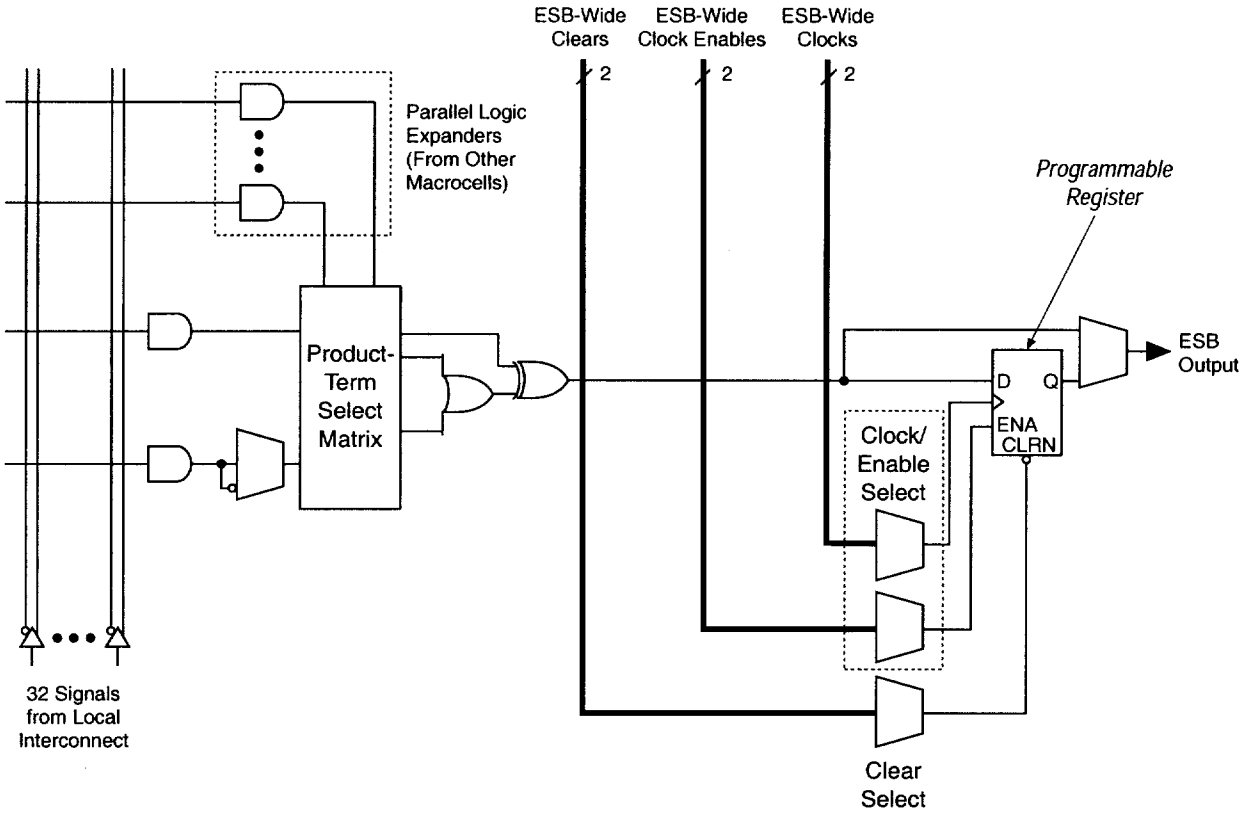
Note:
(1) APEX 20KE devices have four dedicated clocks.

Macrocells

APEX 20K macrocells can be configured individually for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register.

Combinatorial logic is implemented in the product terms. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as parallel expanders to be used to increase the logic available to another macrocell. One product term can be inverted; the Quartus software uses this feature to perform DeMorgan's inversion for more efficient implementation of wide OR functions. The Quartus Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Figure 14 shows the APEX 20K macrocell.

Figure 14. APEX 20K Macrocell



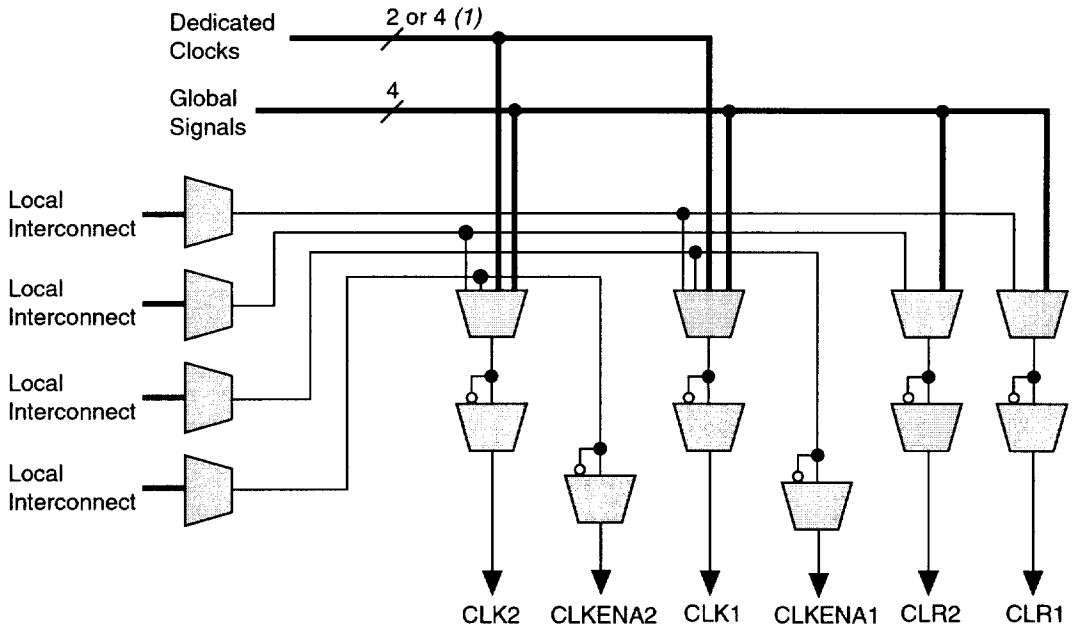
For registered functions, each macrocell register can be programmed individually to implement D, T, JK, or SR operation with programmable clock control. The register can be bypassed for combinatorial operation. During design entry, the designer specifies the desired register type; the Quartus software then selects the most efficient register operation for each registered function to optimize resource utilization. The Quartus software or other synthesis tools can also select the most efficient register operation automatically when synthesizing HDL designs.

Each programmable register can be clocked by one of two ESB-wide clocks. The ESB-wide clocks can be generated from device dedicated clock pins, global signals, or local interconnect. Each clock also has an associated clock enable, generated from the local interconnect. The clock and clock enable signals are related for a particular ESB; any macrocell using a clock also uses the associated clock enable.

If both the rising and falling edges of a clock are used in an ESB, both ESB-wide clock signals are used.

The programmable register also supports an asynchronous clear function. Within the ESB, two asynchronous clears are generated from global signals and the local interconnect. Each macrocell can either choose between the two asynchronous clear signals or choose to not be cleared. Either of the two clear signals can be inverted within the ESB. Figure 15 shows the ESB control logic when implementing product-terms.

Figure 15. ESB Product-Term Mode Control Logic



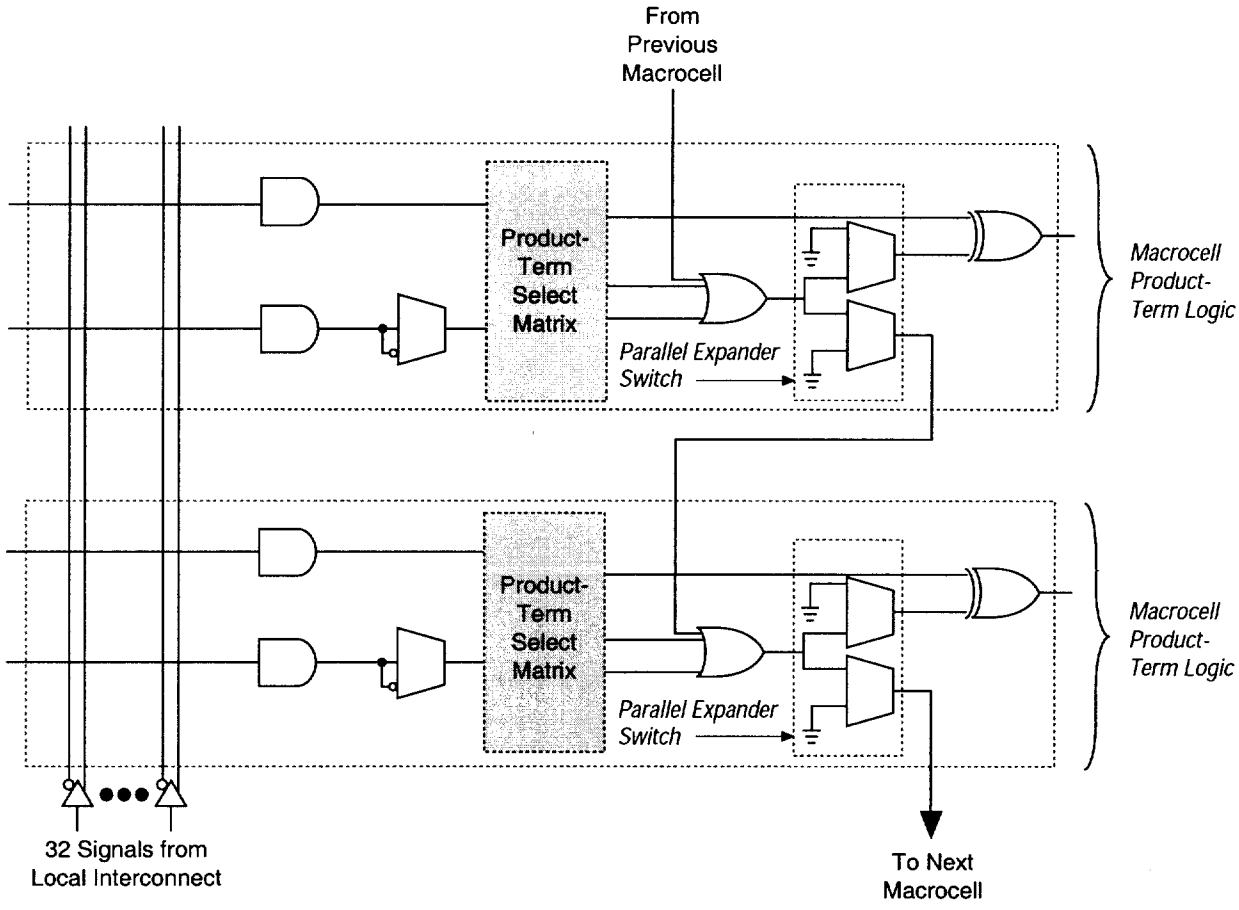
Note:
(1) APEX 20KE devices have four dedicated clocks.

Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 32 product terms to feed the macrocell OR logic directly, with two product terms provided by the macrocell and 30 parallel expanders provided by the neighboring macrocells in the ESB.

The Quartus Compiler can allocate up to 15 sets of up to two parallel expanders per set to the macrocells automatically. Each set of two parallel expanders incurs a small, incremental timing delay. Figure 16 shows the APEX 20K parallel expanders.

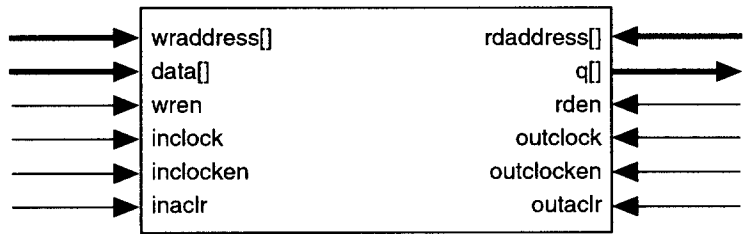
Figure 16. APEX 20K Parallel Expanders



Embedded System Block

The ESB can implement various types of memory blocks, including dual-port RAM, ROM, FIFO, and CAM blocks. The ESB includes input and output registers; the input registers synchronize writes, and the output registers can pipeline designs to improve system performance. The ESB offers a dual-port mode, which supports simultaneous reads and writes at two different clock frequencies. Figure 17 shows the ESB block diagram.

Figure 17. ESB Block Diagram



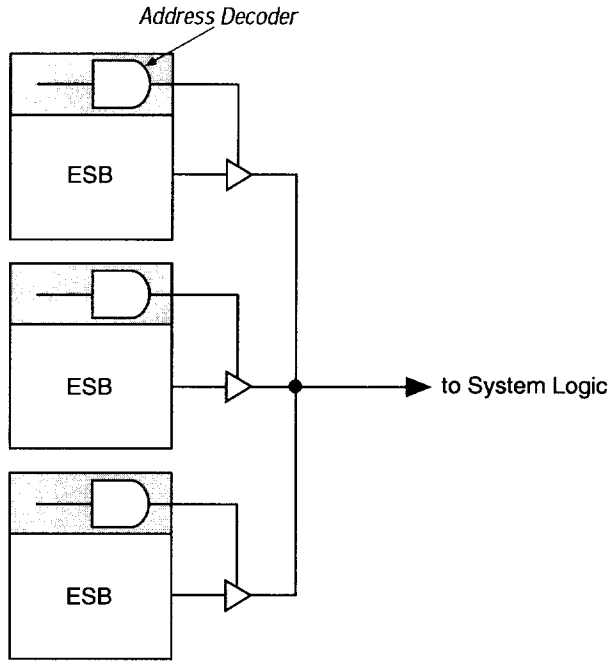
ESBs can implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable (WE) signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the WE signal. In contrast, the ESB's synchronous RAM generates its own WE signal and is self-timed with respect to the global clock. Circuits using the ESB's self-timed RAM must only meet the setup and hold time specifications of the global clock.

ESB inputs are driven by the adjacent local interconnect, which in turn can be driven by the MegaLAB or FastTrack Interconnect. Because the ESB can be driven by the local interconnect, an adjacent LE can drive it directly for fast memory access. ESB outputs drive the MegaLAB and FastTrack Interconnect. In addition, ten ESB outputs, nine of which are unique output lines, drive the local interconnect for fast connection to adjacent LEs or for fast feedback product-term logic.

When implementing memory, each ESB can be configured in any of the following sizes: 128 × 16, 256 × 8, 512 × 4, 1,024 × 2, or 2,048 × 1. By combining multiple ESBs, the Quartus software implements larger memory blocks automatically. For example, two 128 × 16 RAM blocks can be combined to form a 128 × 32 RAM block, and two 512 × 4 RAM blocks can be combined to form a 512 × 8 RAM block. Memory performance does not degrade for memory blocks up to 2,048 words deep. Each ESB can implement a 2,048-word-deep memory; the ESBs are used in parallel, eliminating the need for any external control logic and its associated delays.

To create a high-speed memory block that is more than 2,048 words deep, ESBs drive tri-state lines. Each tri-state line connects all ESBs in a column of MegaLAB structures, and drives the MegaLAB interconnect and row and column FastTrack Interconnect throughout the column. Each ESB incorporates a programmable decoder to activate the tri-state driver appropriately. For instance, to implement 8,192-word-deep memory, four ESBs are used. Eleven address lines drive the ESB memory, and two more drive the tri-state decoder. Depending on which 2,048-word memory page is selected, the appropriate ESB driver is turned on, driving the output to the tri-state line. The Quartus software automatically combines ESBs with tri-state lines to form deeper memory blocks. The internal tri-state control logic is designed to avoid internal contention and floating lines. See Figure 18.

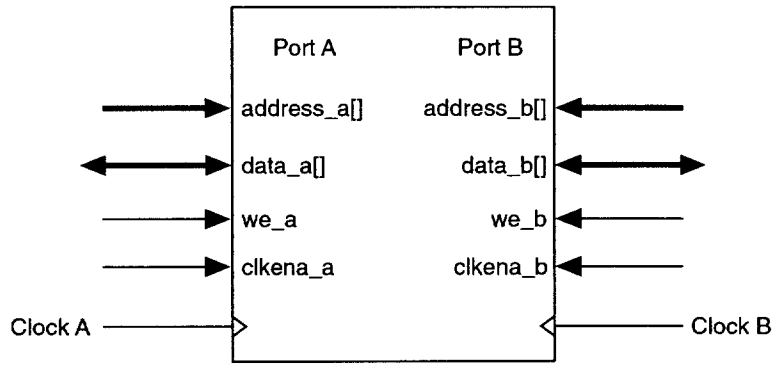
Figure 18. Deep Memory Block Implemented with Multiple ESBs



The ESB implements two forms of dual-port memory: read/write clock mode and input/output clock mode. The ESB can also be used for bidirectional, dual-port memory applications in which two ports read or write simultaneously. To implement this type of dual-port memory, two ESBs are used to support two simultaneous reads or writes.

The ESB can also use Altera megafunctions to implement dual-port RAM applications where both ports can read or write, as shown in Figure 19.

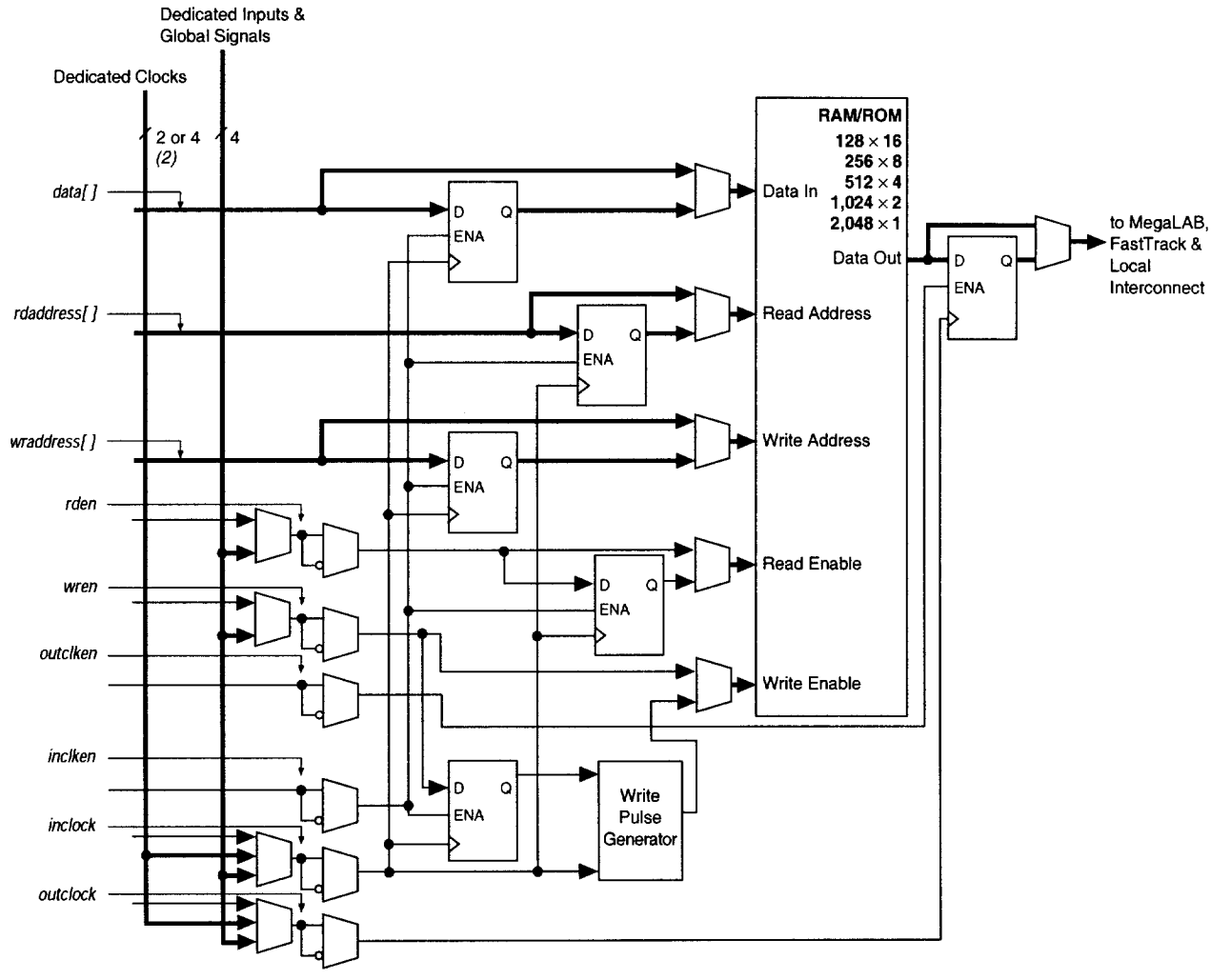
Figure 19. APEX 20K ESB Implementing Dual-Port RAM



Read/Write Clock Mode

The read/write clock mode contains two clocks. One clock controls all registers associated with writing: data input, WE, and write address. The other clock controls all registers associated with reading: read enable (RE), read address, and data output. The ESB also supports clock enable and asynchronous clear signals; these signals also control the read and write registers independently. Read/write clock mode is commonly used for applications where reads and writes occur at different system frequencies. Figure 20 shows the ESB in read/write clock mode.

Figure 20. ESB in Read/Write Clock Mode *Note (1)*

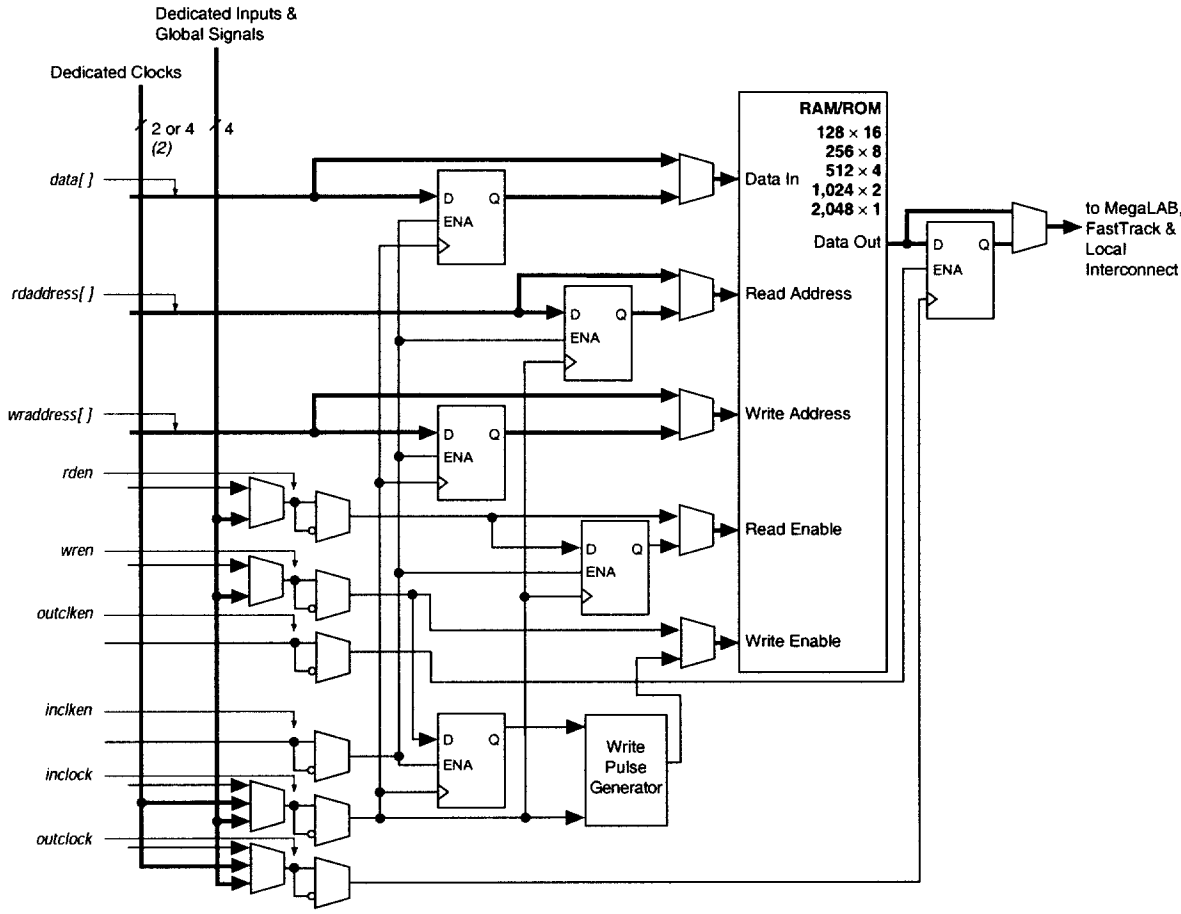


Notes:
(1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.
(2) APEX 20KE devices have four dedicated clocks.

Input/Output Clock Mode

The input/output clock mode contains two clocks. One clock controls all registers for inputs into the ESB: data input, WE, RE, read address, and write address. The other clock controls the ESB data output registers. The ESB also supports clock enable and asynchronous clear signals; these signals also control the reading and writing of registers independently. Input/output clock mode is commonly used for applications where the reads and writes occur at the same system frequency, but require different clock enable signals for the input and output registers. Figure 21 shows the ESB in input/output clock mode.

Figure 21. ESB in Input/Output Clock Mode *Notes (1), (2)*

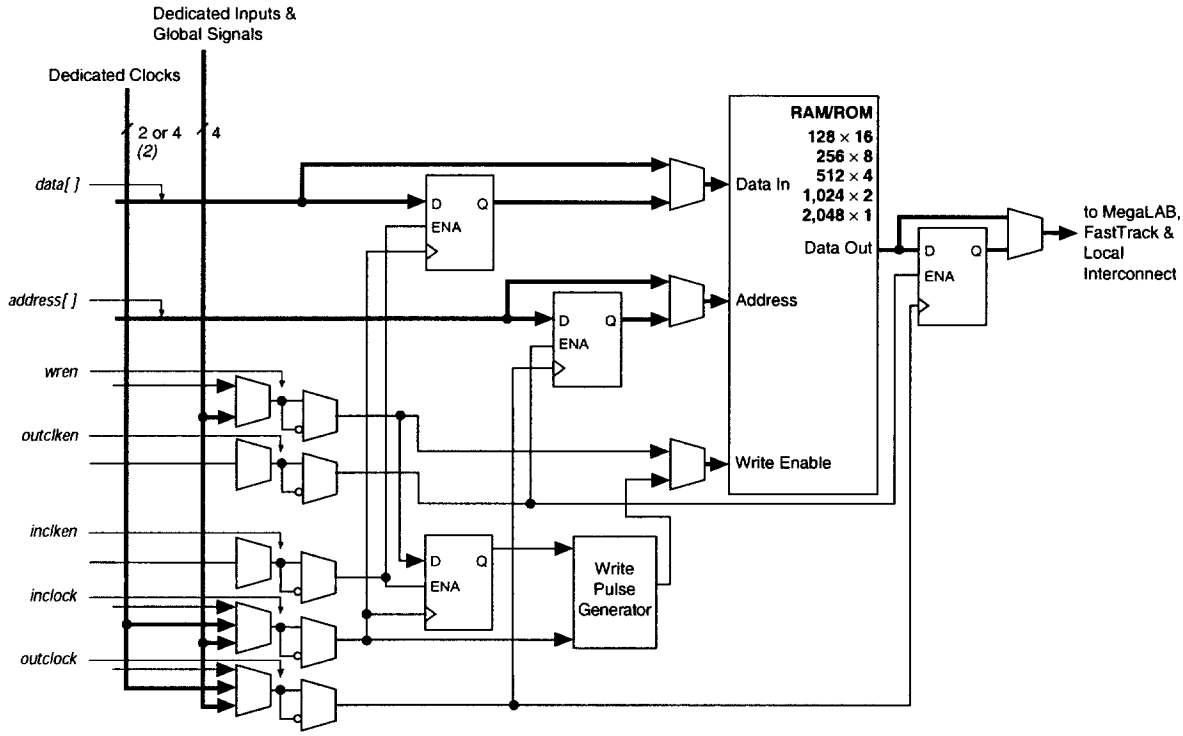


Notes:
(1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.
(2) APEX 20KE devices have four dedicated clocks.

Single-Port Mode

The APEX 20K ESB also supports a single-port mode, which is used when simultaneous reads and writes are not required. See Figure 22.

Figure 22. ESB in Single-Port Mode *Note (1)*



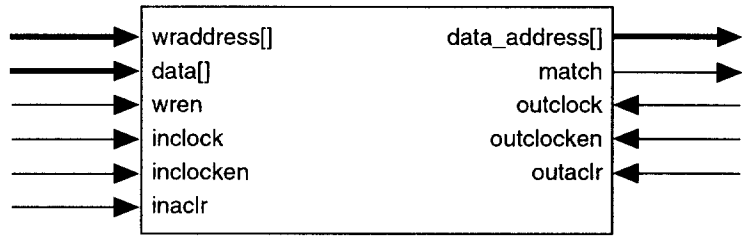
Notes:
(1) All registers can be asynchronously cleared by ESB local interconnect signals, global signals, or the chip-wide reset.
(2) APEX 20KE devices have four dedicated clocks.

Content-Addressable Memory

In APEX 20KE devices, the ESB can implement CAM. CAM can be thought of as the inverse of RAM. When read, RAM outputs the data for a given address. Conversely, CAM outputs an address for a given data word. For example, if the data FA12 is stored in address 14, the CAM outputs 14 when FA12 is driven into it.

CAM is used for high-speed search operations. When searching for data within a RAM block, the search is performed serially. Thus, finding a particular data word can take many cycles. CAM searches all addresses in parallel and outputs the address storing a particular word. When a match is found, a match flag is set high. Figure 23 shows the CAM block diagram.

Figure 23. APEX 20KE CAM Block Diagram



CAM can be used in any application requiring high-speed searches, such as networking, communications, data compression, and cache management.

The APEX 20KE on-chip CAM provides faster system performance than traditional discrete CAM. Integrating CAM and logic into the APEX 20KE device eliminates off-chip and on-chip delays, improving system performance.

When in CAM mode, the ESB implements 32-word, 32-bit CAM. Wider or deeper CAM can be implemented by combining multiple CAMs with some ancillary logic implemented in LEs. The Quartus software combines ESBs and LEs automatically to create larger CAMs.

CAM supports writing "don't care" bits into words of the memory. The "don't-care" bit can be used as a mask for CAM comparisons; any bit set to "don't-care" has no effect on matches.

The output of the CAM can be encoded or unencoded. When encoded, the ESB outputs an encoded address of the data's location. For instance, if the data is located in address 12, the ESB output is 12. When unencoded, the ESB uses its 16 outputs to show the location of the data over two clock cycles. In this case, if the data is located in address 12, the 12th output line goes high. When using unencoded outputs, two clock cycles are required to read the output because a 16-bit output bus is used to show the status of 32 words.

The encoded output is better suited for designs that ensure duplicate data is not written into the CAM. If duplicate data is written into two locations, the CAM's output will be incorrect. If the CAM may contain duplicate data, the unencoded output is a better solution; CAM with unencoded outputs can distinguish multiple data locations.

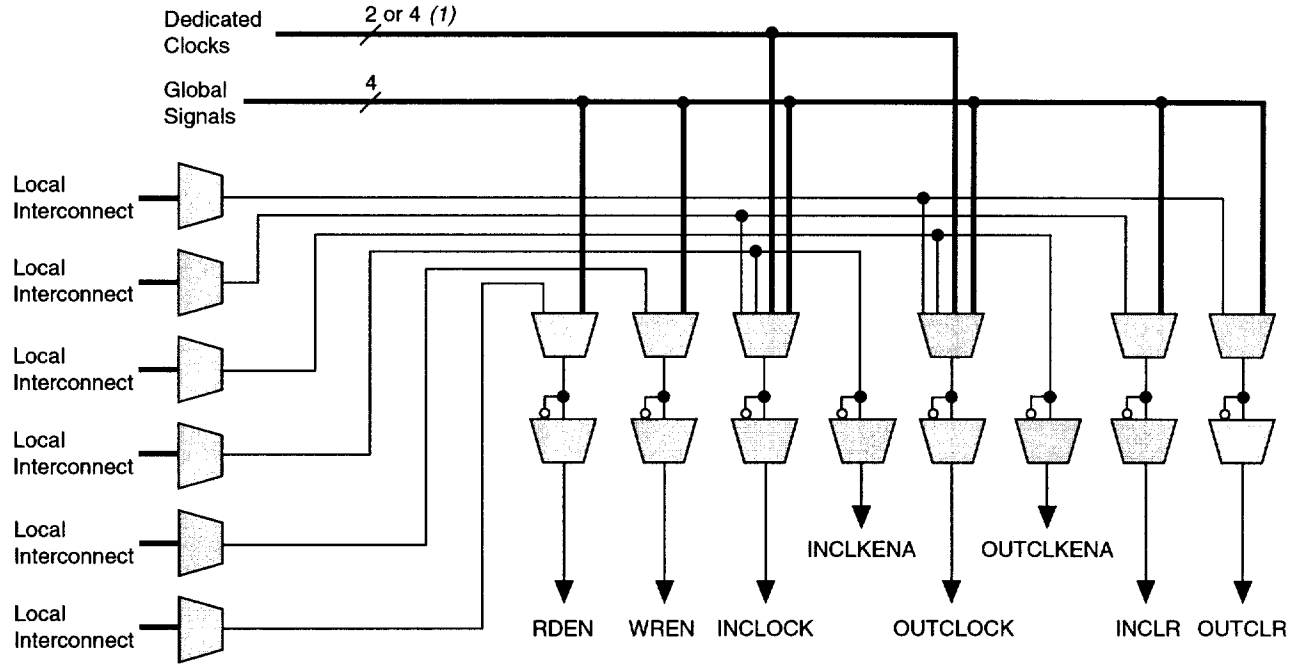
CAM can be pre-loaded with data during configuration, or it can be written during system operation. In most cases, two clock cycles are required to write each word into CAM. When "don't-care" bits are used, a third clock cycle is required.

For more information on APEX 20KE devices and CAM, see *Application Note 119 (Implementing High-Speed Search Applications with APEX CAM).*

Driving Signals to the ESB

ESBs provide flexible options for driving control signals. Different clocks can be used for the ESB inputs and outputs. Registers can be inserted independently on the data input, data output, read address, write address, WE, and RE signals. The global signals and the local interconnect can drive the WE and RE signals. The global signals, dedicated clock pins, and local interconnect can drive the ESB clock signals. Because the LEs drive the local interconnect, the LEs can control the WE and RE signals and the ESB clock, clock enable, and asynchronous clear signals. Figure 24 shows the ESB control signal generation logic.

Figure 24. ESB Control Signal Generation



Note:
(1) APEX 20KE devices have four dedicated clocks.

An ESB is fed by the local interconnect, which is driven by adjacent LEs (for high-speed connection to the ESB) or the MegaLAB interconnect. The ESB can drive the local, MegaLAB, or FastTrack Interconnect routing structure to drive LEs and IOEs in the same MegaLAB structure or anywhere in the device.

Implementing Logic in ROM

In addition to implementing logic with product terms, the ESB can implement logic functions when it is programmed with a read-only pattern during configuration, creating a large LUT. With LUTs, combinatorial functions are implemented by looking up the results, rather than by computing them. This implementation of combinatorial functions can be faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of ESBs. The large capacity of ESBs enables designers to implement complex functions in one logic level without the routing delays associated with linked LEs or distributed RAM blocks. Parameterized functions such as LPM functions can take advantage of the ESB automatically. Further, the Quartus software can implement portions of a design with ESBs where appropriate.

Programmable Speed/Power Control

APEX 20K ESBs offer a high-speed mode that supports very fast operation on an ESB-by-ESB basis. When high speed is not required, this feature can be turned off to reduce the ESB's power dissipation by up to 50%. ESBs that run at low power incur a nominal timing delay adder. This Turbo Bit™ option is available for ESBs that implement product-term logic or memory functions. An ESB that is not used will be powered down so that it does not consume DC current.

Designers can program each ESB in the APEX 20K device for either high-speed or low-power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths operate at reduced power.

I/O Structure

The APEX 20K IOE contains a bidirectional I/O buffer and a register that can be used either as an input register for external data requiring fast setup times, or as an output register for data requiring fast clock-to-output performance. IOEs can be used as input, output, or bidirectional pins. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing. The Quartus Compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. Because the APEX 20K IOE offers one output enable per pin, the Quartus Compiler can emulate open-drain operation efficiently.

The APEX 20K IOE includes programmable delays that can be activated to ensure zero hold times, minimum clock-to-output times, input IOE register-to-core register transfers, or core-to-output IOE register transfers. A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay.

Table 10 describes the APEX 20K programmable delays and their logic options in the Quartus software.

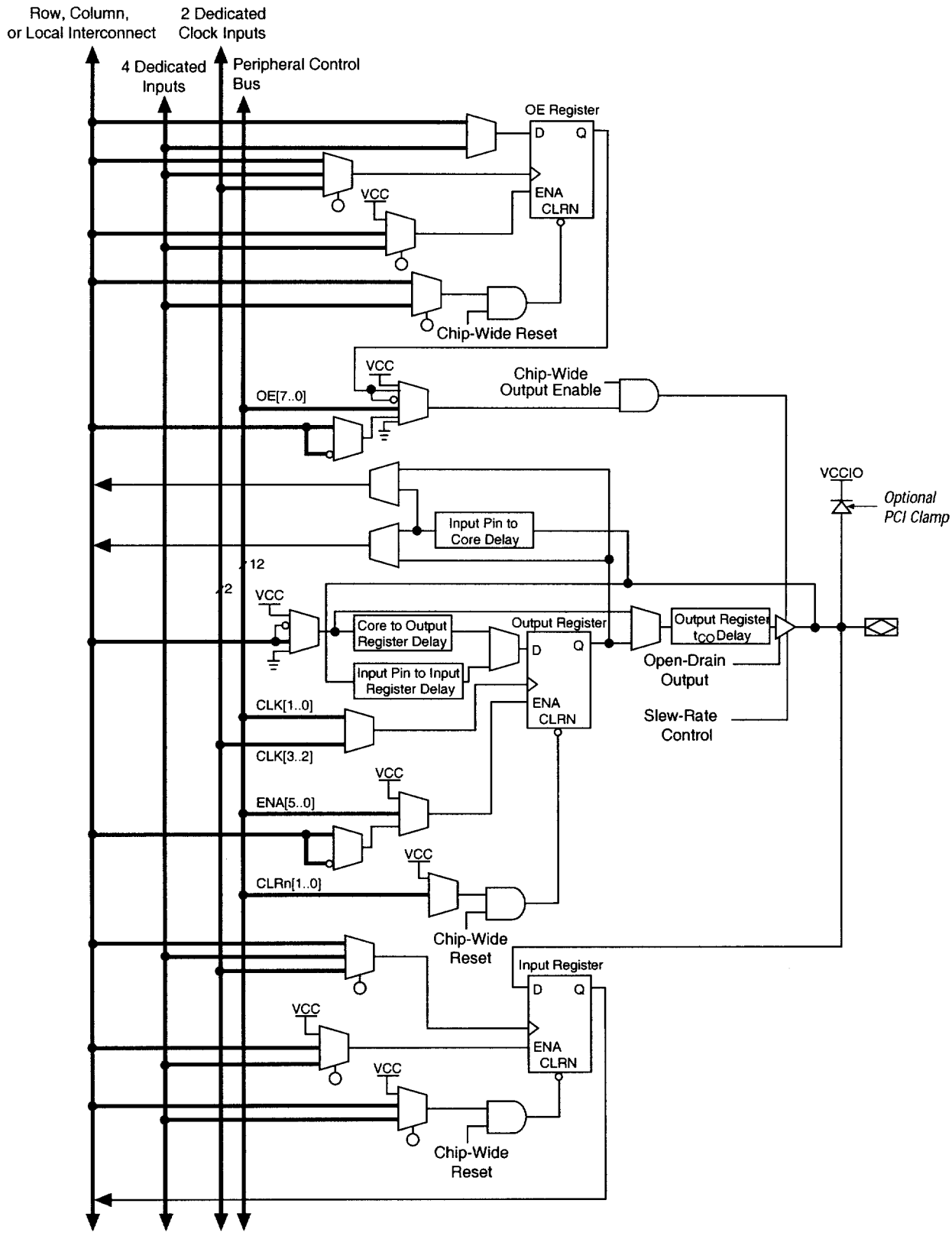
Table 10. APEX 20K Programmable Delay Chains

Programmable Delays	Quartus Logic Option
Input pin to core delay	Decrease input delay to internal cells
Input pin to input register delay	Decrease input delay to input register
Core to output register delay	Decrease input delay to output register
Output register t_{CO} delay	Increase delay to output pin

The Quartus Compiler can program these delays automatically to minimize setup time while providing a zero hold time. Figure 25 shows how fast bidirectional I/Os are implemented in APEX 20K devices.

The register in the APEX 20K IOE can be programmed to power-up high or low after configuration is complete. If it is programmed to power-up low, an asynchronous clear can control the register. If it is programmed to power-up high, the register cannot be asynchronously cleared or preset. This feature is useful for cases where the APEX 20K device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

Figure 25. APEX 20K Bidirectional I/O Registers *Note (1)*



Note:

(1) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin.

APEX 20KE devices include an enhanced IOE, which drives the FastRow interconnect. The FastRow interconnect connects a column I/O pin directly to the LAB local interconnect within two MegaLAB structures. This feature provides fast setup times for pins that drive high fan-outs with complex logic, such as PCI designs. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing. The APEX 20KE IOE also includes direct support for open-drain operation, giving faster clock-to-output for open-drain signals. Some programmable delays in the APEX 20KE IOE offer multiple levels of delay to fine-tune setup and hold time requirements. The Quartus Compiler can set these delays automatically to minimize setup time while providing a zero hold time.

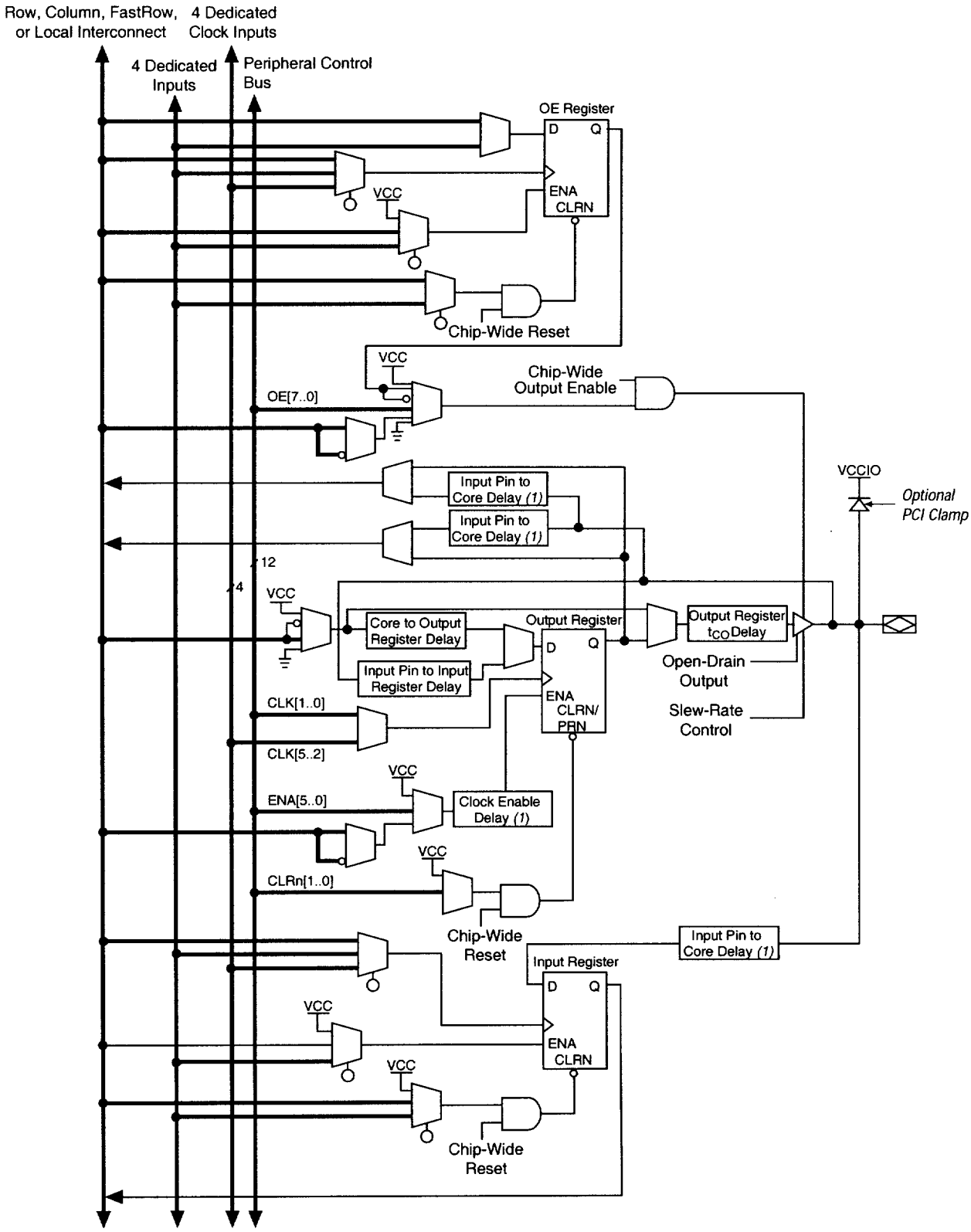
Table 11 describes the APEX 20KE programmable delays and their logic options in the Quartus software.

Table 11. APEX 20KE Programmable Delay Chains

Programmable Delays	Quartus Logic Option
Input Pin to Core Delay	Decrease input delay to internal cells
Input Pin to Input Register Delay	Decrease input delay to input registers
Core to Output Register Delay	Decrease input delay to output register
Output Register t_{CO} Delay	Increase delay to output pin
Clock Enable Delay	Increase clock enable delay

The register in the APEX 20KE IOE can be programmed to power-up high or low after configuration is complete. If it is programmed to power-up low, an asynchronous clear can control the register. If it is programmed to power-up high, an asynchronous preset can control the register. Figure 26 shows how fast bidirectional I/O pins are implemented in APEX 20KE devices. This feature is useful for cases where the APEX 20KE device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

Figure 26. APEX 20KE Bidirectional I/O Registers *Notes (1), (2)*



Notes:
(1) This programmable delay has four settings: off and three levels of delay.
(2) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin.

Each IOE drives a row, column, MegaLAB, or local interconnect when used as an input or bidirectional pin. A row IOE can drive a local, MegaLAB, row, and column interconnect; a column IOE can drive the column interconnect. Figure 27shows how a row IOE connects to the interconnect.

Figure 27. Row IOE Connection to the Interconnect

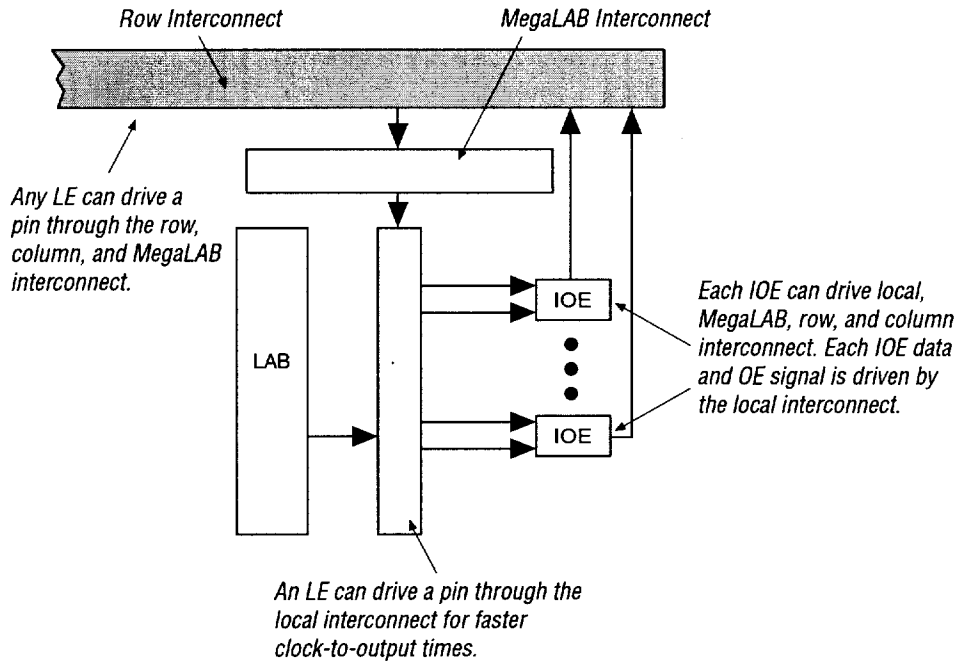
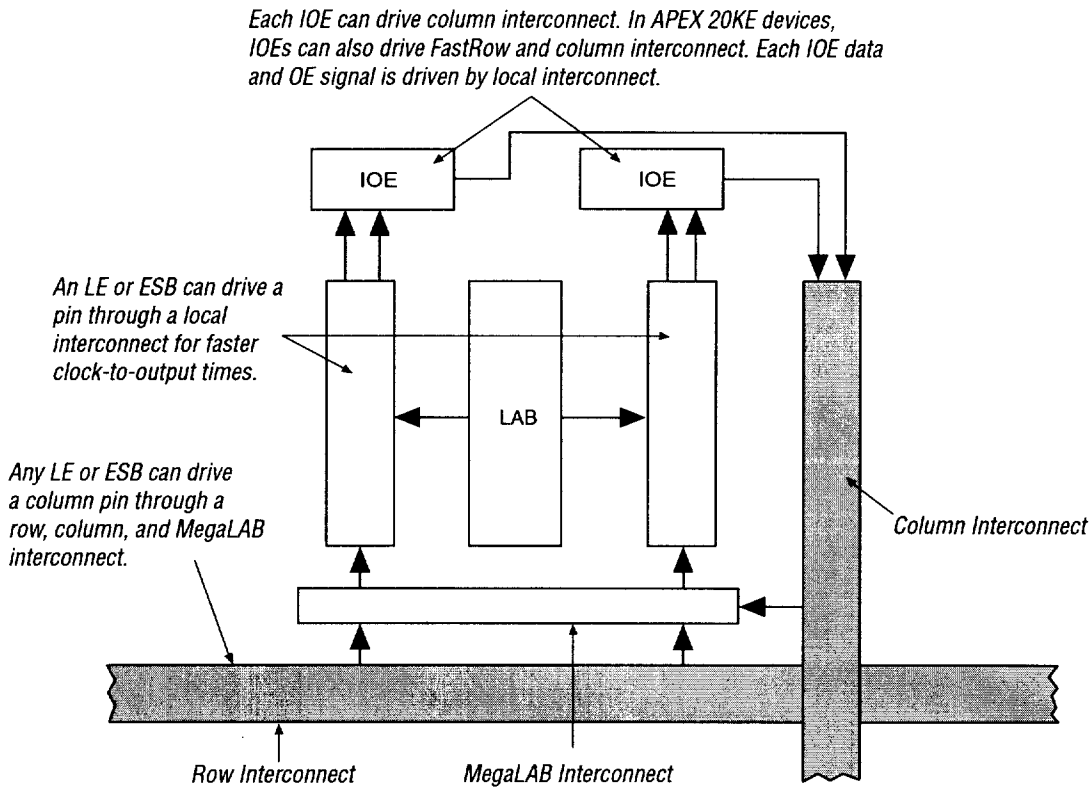


Figure 28 shows how a column IOE connects to the interconnect.

Figure 28. Column IOE Connection to the Interconnect



Dedicated Fast I/Os

APEX 20KE devices incorporate an enhancement to support bidirectional pins with high internal fanout such as PCI control signals. These pins are called Dedicated Fast I/Os (FAST1, FAST2, FAST3, and FAST4) and replace dedicated inputs. These pins can be used for fast clock, clear, or high fanout logic signal distribution. They also can drive out. The Dedicated Fast I/O pin data output and tri-state control are driven by local interconnect from the adjacent MegaLAB for high speed.

Advanced I/O Standard Support

APEX 20KE IOEs support the following I/O standards: LVTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, 3.3-V PCI, PCI-X, 3.3-V AGP, LVDS, LVPECL, GTL+, CTT, HSTL Class I, SSTL-3 Class I and II, and SSTL-2 Class I and II.

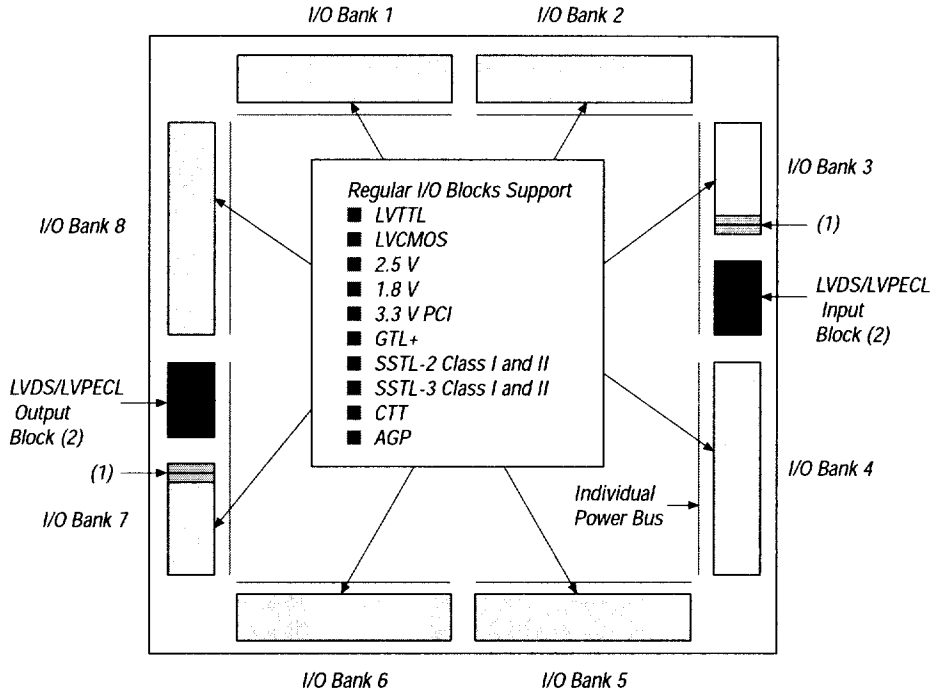
For more information on I/O standards supported by APEX 20KE devices, see *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

The APEX 20KE device contains eight I/O banks. In QFP packages, the banks are linked to form four I/O banks. The I/O banks directly support all standards except LVDS and LVPECL. All I/O banks can support LVDS and LVPECL with the addition of external resistors. In addition, one block within a bank contains circuitry to support high-speed True-LVDS and LVPECL inputs, and another block within a bank supports high-speed True-LVDS and LVPECL outputs. The LVDS blocks support all of the I/O standards. Each I/O bank has its own VCCIO pins. A single device can support 1.8-V, 2.5-V, and 3.3-V interfaces; each bank can support a different standard independently. Each bank can also use a separate V_{REF} level so that each bank can support any of the terminated standards (such as SSTL-3) independently. Within a bank, any one of the terminated standards can be supported. EP20K300E and larger APEX 20KE devices support the LVDS interface for data pins (smaller devices support LVDS clock pins, but not data pins). All EP20K300E and larger devices support the LVDS interface for data pins up to 155 Mbit per channel; EP20K400E devices and larger with an X-suffix on the ordering code add a serializer/deserializer circuit and PLL for support up to 840 Mbit per channel.

Each bank can support multiple standards with the same VCCIO for output pins. Each bank can support one voltage-referenced I/O standard, but it can support multiple I/O standards with the same VCCIO voltage level. For example, when VCCIO is 3.3 V, a bank can support LVTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs.

When the LVDS banks are not used for LVDS I/Os, they support all of the other I/O standards. Figure 29 shows the arrangement of the APEX 20KE I/O banks.

Figure 29. APEX 20KE I/O Banks



Notes:

(1) The first two I/O pins that border the LVDS blocks can only be used for input to maintain an acceptable noise level on the V_{CCIO} plane.

(2) If the LVDS input and output blocks are not used for LVDS, they can support all of the I/O standards and can be used as input, output, or bidirectional pins with V_{CCIO} set to 3.3 V, 2.5 V, or 1.8 V.

Power Sequencing & Hot Socketing

Because APEX 20K devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Therefore, the V_{CCIO} and V_{CCINT} power planes may be powered in any order.

Signals can be driven into APEX 20K devices before and during power-up without damaging the device. In addition, APEX 20K devices do not drive out during power-up. Once operating conditions are reached and the device is configured, APEX 20K devices operate as specified by the user.

MultiVolt I/O Interface

The APEX architecture supports the MultiVolt I/O interface feature, which allows APEX devices in all packages to interface with systems of different supply voltages. The devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The APEX 20K VCCINT pins must always be connected to a 2.5 V power supply. With a 2.5-V V_{CCINT} level, input pins are 2.5-V and 3.3-V tolerant. The devices, identified by a "V" suffix following the speed grade in the ordering code (e.g., EP20K400BC652-1V), are 5.0-V tolerant. The VCCIO pins can be connected to either a 2.5-V or 3.3-V power supply, depending on the output requirements. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems.

Table 12 summarizes 5.0-V tolerant APEX 20K MultiVolt I/O support.

Table 12. 5.0-V Tolerant APEX 20K MultiVolt I/O Support

V_{CCIO} (V)	Input Signals (V)			Output Signals (V)		
	2.5	3.3	5.0	2.5	3.3	5.0
2.5	✓	✓(1)	✓(1), (2)	✓		
3.3	✓	✓	✓(1), (2)	✓(3)	✓	✓

Notes:
(1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}.
(2) APEX 20K devices with a "V" suffix are 5.0-V tolerant.
(3) When V_{CCIO} = 3.3 V, an APEX 20K device can drive a 2.5-V device with 3.3-V tolerant inputs.

Open-drain output pins on 5.0-V tolerant APEX 20K devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a V_{IH} of 3.5 V. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

APEX 20KE devices also support the MultiVolt I/O interface feature. The APEX 20KE VCCINT pins must always be connected to a 1.8-V power supply. With a 1.8-V V_{CCINT} level, input pins are 1.8-V, 2.5-V, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.8-V, 2.5-V, or 3.3-V power supply, depending on the I/O standard requirements. When the VCCIO pins are connected to a 1.8-V power supply, the output levels are compatible with 1.8-V systems. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and compatible with 3.3-V or 5.0-V systems. An APEX 20KE device is 5.0-V tolerant with the addition of a resistor.

Table 13 summarizes APEX 20KE MultiVolt I/O support.

Table 13. APEX 20KE MultiVolt I/O Support

V_{CCIO} (V)	Input Signals (V)				Output Signals (V)			
	1.8	2.5	3.3	5.0	1.8	2.5	3.3	5.0
1.8	✓	✓(1)	✓(1)		✓			
2.5		✓	✓(1)			✓		
3.3		✓	✓	✓(3)		✓(2)	✓	✓

Notes:

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}, except for the 5.0-V input case.

(2) When VCCIO = 3.3 V, an APEX 20KE device can drive a 2.5-V device with 3.3-V tolerant inputs.

(3) An APEX 20KE device can be made 5.0-V tolerant with the addition of an external resistor.

ClockLock & ClockBoost Features

APEX 20K devices support the ClockLock and ClockBoost clock management features, which are implemented with PLLs. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by sharing resources within the device. The ClockBoost circuitry allows the designer to distribute a low-speed clock and multiply that clock on-device. APEX 20K devices include a high-speed clock tree; unlike ASICs, the user does not have to design and optimize the clock tree. The ClockLock and ClockBoost features work in conjunction with the APEX 20K device's high-speed clock to provide significant improvements in system performance and band-width. Devices with an X-suffix on the ordering code include the ClockLock circuit.

The ClockLock and ClockBoost features in APEX 20K devices are enabled through the Quartus software. External devices are not required to use these features.

For designs that require both a multiplied and non-multiplied clock, the clock trace on the board can be connected to CLK2p. Table 14 shows the combinations supported by the ClockLock and ClockBoost circuitry. The CLK2p pin can feed both the ClockLock and ClockBoost circuitry in the APEX 20K device. However, when both circuits are used, the other clock pin (CLK1p) cannot be used.

Table 14. Multiplication Factor Combinations

Clock 1	Clock 2
×1	×1
×1, ×2	×2
×1, ×2, ×4	×4

APEX 20KE ClockLock Feature

APEX 20KE devices include an enhanced ClockLock feature set. These devices include up to four PLLs, which can be used independently. Two PLLs are designed for either general-purpose use or LVDS use (on devices that support LVDS I/O pins). The remaining two PLLs are designed for general-purpose use. The EP20K200E and smaller devices have two PLLs; the EP20K300E and larger devices have four PLLs.

The following sections describe some of the features offered by the APEX 20KE PLLs.

External PLL Feedback

The ClockLock circuit's output can be driven off-chip to clock other devices in the system; further, the feedback loop of the PLL can be routed off-chip. This feature allows the designer to exercise fine control over the I/O interface between the APEX 20KE device and another high-speed device, such as SDRAM.

Clock Multiplication

The APEX 20KE ClockBoost circuit can multiply or divide clocks by a programmable number. The clock can be multiplied by $m/(n \times k)$, where m, and k range from 2 to 160 and n ranges from 1 to 16. Clock multiplication and division can be used for time-domain multiplexing and other functions, which can reduce design LE requirements.

Clock Phase & Delay Adjustment

The APEX 20KE ClockShift feature allows the clock phase and delay to be adjusted. The clock phase can be adjusted by 90° steps. The clock delay can be adjusted to increase or decrease the clock delay by an arbitrary amount, up to one clock period.

LVDS Support

Two PLLs are designed to support the LVDS interface. When using LVDS, the I/O clock runs at a slower rate than the data transfer rate. Thus, PLLs are used to multiply the I/O clock internally to capture the LVDS data. For example, an I/O clock may run at 105 MHz to support 840 megabits per second (Mbps) LVDS data transfer. In this example, the PLL multiplies the incoming clock by eight to support the high-speed data transfer. You can use PLLs in EP20K400E and larger devices for high-speed LVDS interfacing.

Lock Signals

The APEX 20KE ClockLock circuitry supports individual LOCK signals. The LOCK signal drives high when the ClockLock circuit has locked onto the input clock. The LOCK signals are optional for each ClockLock circuit; when not used, they are I/O pins.

ClockLock & ClockBoost Timing Parameters

For the ClockLock and ClockBoost circuitry to function properly, the incoming clock must meet certain requirements. If these specifications are not met, the circuitry may not lock onto the incoming clock, which generates an erroneous clock within the device. The clock generated by the ClockLock and ClockBoost circuitry must also meet certain specifications. If the incoming clock meets these requirements during configuration, the APEX 20K ClockLock and ClockBoost circuitry will lock onto the clock during configuration. The circuit will be ready for use immediately after configuration. In APEX 20KE devices, the clock input standard is programmable, so the PLL cannot respond to the clock until the device is configured. The PLL locks onto the input clock as soon as configuration is complete. Figure 30 shows the incoming and generated clock specifications.

For more information on ClockLock and ClockBoost circuitry, see *Application Note 115: Using the ClockLock and ClockBoost PLL Features in APEX Devices.*

Figure 30. Specifications for the Incoming & Generated Clocks

The t_I parameter refers to the nominal input clock period; the t_O parameter refers to the nominal output clock period.

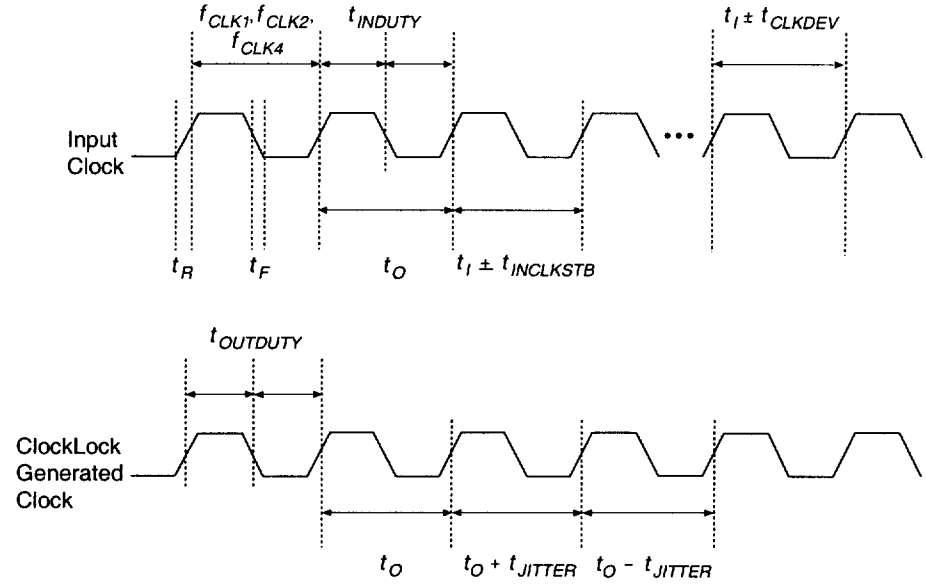


Table 15 summarizes the APEX 20K ClockLock and ClockBoost parameters for -1 speed grade devices.

Table 15. APEX 20K ClockLock & ClockBoost Parameters for -1 Speed-Grade Devices (Part 1 of 2)

Symbol	Parameter	Min	Max	Unit
f_{OUT}	Output frequency	25	180	MHz
f_{CLK1} *(1)*	Input clock frequency (ClockBoost clock multiplication factor equals 1)	25	180 *(1)*	MHz
f_{CLK2}	Input clock frequency (ClockBoost clock multiplication factor equals 2)	16	90	MHz
f_{CLK4}	Input clock frequency (ClockBoost clock multiplication factor equals 4)	10	48	MHz
$t_{OUTDUTY}$	Duty cycle for ClockLock/ClockBoost-generated clock	40	60	%
f_{CLKDEV}	Input deviation from user specification in the Quartus software (ClockBoost clock multiplication factor equals 1) *(2)*		25,000 *(3)*	PPM
t_R	Input rise time		5	ns
t_F	Input fall time		5	ns

Table 15. APEX 20K ClockLock & ClockBoost Parameters for -1 Speed-Grade Devices (Part 2 of 2)

Symbol	Parameter	Min	Max	Unit
t_{LOCK}	Time required for ClockLock/ClockBoost to acquire lock *(4)*		10	µs
t_{SKEW}	Skew delay between related ClockLock/ClockBoost-generated clocks		500	ps
t_{JITTER}	Jitter on ClockLock/ClockBoost-generated clock *(5)*		200	ps
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)		50	ps

Notes:
(1) The PLL input frequency range for the EP20K100-1X device for 1x multiplication is 25 MHz to 175 MHz.
(2) All input clock specifications must be met. The PLL may not lock onto an incoming clock if the clock specifications are not met, creating an erroneous clock within the device.
(3) During device configuration, the ClockLock and ClockBoost circuitry is configured first. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration, because the lock time is less than the configuration time.
(4) The jitter specification is measured under long-term observation.
(5) If the input clock stability is 100 ps, t_{JITTER} is 250 ps.

Table 16 summarizes the APEX 20K ClockLock and ClockBoost parameters for -2 speed grade devices.

Table 16. APEX 20K ClockLock & ClockBoost Parameters for -2 Speed Grade Devices (Part 1 of 2)

Symbol	Parameter	Min	Max	Unit
f_{OUT}	Output frequency	25	170	MHz
f_{CLK1}	Input clock frequency (ClockBoost clock multiplication factor equals 1)	25	170	MHz
f_{CLK2}	Input clock frequency (ClockBoost clock multiplication factor equals 2)	16	80	MHz
f_{CLK4}	Input clock frequency (ClockBoost clock multiplication factor equals 4)	10	34	MHz
$t_{OUTDUTY}$	Duty cycle for ClockLock/ClockBoost-generated clock	40	60	%
f_{CLKDEV}	Input deviation from user specification in the Quartus software (ClockBoost clock multiplication factor equals one) *(1)*		25,000 *(2)*	PPM
t_R	Input rise time		5	ns
t_F	Input fall time		5	ns

Table 16. APEX 20K ClockLock & ClockBoost Parameters for -2 Speed Grade Devices (Part 2 of 2)

Symbol	Parameter	Min	Max	Unit
t_{LOCK}	Time required for ClockLock/ ClockBoost to acquire lock *(3)*		10	µs
t_{SKEW}	Skew delay between related ClockLock/ ClockBoost-generated clock	500	500	ps
t_{JITTER}	Jitter on ClockLock/ ClockBoost-generated clock *(4)*		200	ps
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)		50	ps

Notes:

(1) To implement the ClockLock and ClockBoost circuitry with the Quartus software, designers must specify the input frequency. The Quartus software tunes the PLL in the ClockLock and ClockBoost circuitry to this frequency. The f_{CLKDEV} parameter specifies how much the incoming clock can differ from the specified frequency during device operation. Simulation does not reflect this parameter.

(2) Twenty-five thousand parts per million (PPM) equates to 2.5% of input clock period.

(3) During device configuration, the ClockLock and ClockBoost circuitry is configured before the rest of the device. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration because the t_{LOCK} value is less than the time required for configuration.

(4) The t_{JITTER} specification is measured under long-term observation.

Tables 17 and 18 summarize the ClockLock and ClockBoost parameters for APEX 20KE devices.

Table 17. APEX 20KE ClockLock & ClockBoost Parameters *Note (1)*

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_R	Input rise time				5	ns
t_F	Input fall time				5	ns
t_{INDUTY}	Input duty cycle		40		60	%
$t_{INJITTER}$	Input jitter peak-to-peak				2% of input period	peak-to-peak
$t_{OUTJITTER}$	Jitter on ClockLock or ClockBoost-generated clock				0.35% of output period	RMS
$t_{OUTDUTY}$	Duty cycle for ClockLock or ClockBoost-generated clock		45		55	%
t_{LOCK} *(2), (3)*	Time required for ClockLock or ClockBoost to acquire lock				40	µs

Table 18. APEX 20KE Clock Input and Output Parameters *Note (1)*

Symbol	Parameter	I/O Standard	-1x Speed Grade		-2x Speed Grade		Units
			Min	Max	Min	Max	
f_{VCO} (4)	Voltage controlled oscillator operating range		200	500	200	500	MHz
f_{CLOCK0}	Clock0 PLL output frequency for internal use		1.5	335	1.5	200	MHz
f_{CLOCK1}	Clock1 PLL output frequency for internal use		20	335	20	200	MHz
f_{CLOCK0_EXT}	Output clock frequency for external clock0 output	3.3V LVTTL	1.5	245	1.5	226	MHz
		2.5V LVTTL	1.5	234	1.5	221	MHz
		1.8V LVTTL	1.5	223	1.5	216	MHz
		GTL+	1.5	205	1.5	193	MHz
		SSTL2 Class I	1.5	158	1.5	157	MHz
		SSTL2 Class II	1.5	142	1.5	142	MHz
		SSTL3 Class I	1.5	166	1.5	162	MHz
		SSTL3 Class II	1.5	149	1.5	146	MHz
		LVDS	1.5	420	1.5	350	MHz
f_{CLOCK1_EXT}	Output clock frequency for external clock1 output	3.3V LVTTL	20	245	20	226	MHz
		2.5V LVTTL	20	234	20	221	MHz
		1.8V LVTTL	20	223	20	216	MHz
		GTL+	20	205	20	193	MHz
		SSTL2 Class I	20	158	20	157	MHz
		SSTL2 Class II	20	142	20	142	MHz
		SSTL3 Class I	20	166	20	162	MHz
		SSTL3 Class II	20	149	20	146	MHz
		LVDS	20	420	20	350	MHz
f_{IN}	Input clock frequency	3.3V LVTTL	1.5	290	1.5	257	MHz
		2.5V LVTTL	1.5	281	1.5	250	MHz
		1.8V LVTTL	1.5	272	1.5	243	MHz
		GTL+	1.5	303	1.5	261	MHz
		SSTL2 Class I	1.5	291	1.5	253	MHz
		SSTL2 Class II	1.5	291	1.5	253	MHz
		SSTL3 Class I	1.5	300	1.5	260	MHz
		SSTL3 Class II	1.5	300	1.5	260	MHz
		LVDS	1.5	420	1.5	350	MHz

Notes:

(1) All input clock specifications must be met. The PLL may not lock onto an incoming clock if the clock specifications are not met, creating an erroneous clock within the device.

(2) The lock time is 40 µs max or 2000 input clock cycles, whichever occurs first.

(3) Before configuration, the PLL circuits are disable and powered down. During configuration, the PLLs are still disabled. The PLLs begin to lock once the device is in the user mode. If the clock enable feature is used, lock begins once the CLKLK_ENA pin goes high in user mode.

(4) The PLL VCO operating range is 200 MHz <= fVCO <= 840 MHz for LVDS mode.

SignalTap Embedded Logic Analyzer

APEX 20K devices include device enhancements to support the SignalTap embedded logic analyzer. By including this circuitry, the APEX 20K device provides the ability to monitor design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry; a designer can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages such as FineLine BGA packages because adding a connection to a pin during the debugging process can be difficult after a board is designed and manufactured.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All APEX 20K devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. APEX 20K devices can also use the JTAG port for configuration with the Quartus software or with hardware using either Jam Files (**.jam**) or Jam Byte-Code Files (**.jbc**). Finally, APEX 20K devices use the JTAG port to monitor the logic operation of the device with the SignalTap embedded logic analyzer. APEX 20K devices support the JTAG instructions shown in Table 19.

Table 19. APEX 20K JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap embedded logic analyzer.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
ICR Instructions	Used when configuring an APEX 20K device via the JTAG port with a MasterBlaster or ByteBlasterMV download cable, or when using a Jam File or Jam Byte-Code File via an embedded processor.
SignalTap Instructions	Monitors internal device operation with the SignalTap embedded logic analyzer.

The APEX 20K device instruction register length is 10 bits. The APEX 20K device USERCODE register length is 32 bits. Tables 20 and 21show the boundary-scan register length and device IDCODE information for APEX 20K devices.

Table 20. APEX 20K Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP20K30E	420
EP20K60E	654
EP20K100	786
EP20K100E	774
EP20K160E	1,176
EP20K200	1,164
EP20K200E	1,188
EP20K300E	1,266
EP20K400	1,536
EP20K400E	1,506
EP20K600E	1,866
EP20K1000E	2,190
EP20K1500E	2,502

Table 21. 32-Bit APEX 20K Device IDCODE

Device	IDCODE (32 Bits) *(1)*			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	1 (1 Bit) *(2)*
EP20K30E	0000	1000 0000 0011 0000	000 0110 1110	1
EP20K60E	0000	1000 0000 0110 0000	000 0110 1110	1
EP20K100	0000	0000 0100 0001 0110	000 0110 1110	1
EP20K100E	0000	1000 0001 0000 0000	000 0110 1110	1
EP20K160E	0000	1000 0001 0110 0000	000 0110 1110	1
EP20K200	0000	0000 1000 0011 0010	000 0110 1110	1
EP20K200E	0000	1000 0010 0000 0000	000 0110 1110	1
EP20K300E	0000	1000 0011 0000 0000	000 0110 1110	1
EP20K400	0000	0001 0110 0110 0100	000 0110 1110	1
EP20K400E	0000	1000 0100 0000 0000	000 0110 1110	1
EP20K600E	0000	1000 0110 0000 0000	000 0110 1110	1
EP20K1000E	0000	1001 0000 0000 0000	000 0110 1110	1
EP20K1500E	0000	1001 0101 0000 0000	000 0110 1110	1

Notes:
(1) The most significant bit (MSB) is on the left.
(2) The IDCODE's least significant bit (LSB) is always 1.

Figure 31 shows the timing requirements for the JTAG signals.

Figure 31. APEX 20K JTAG Waveforms

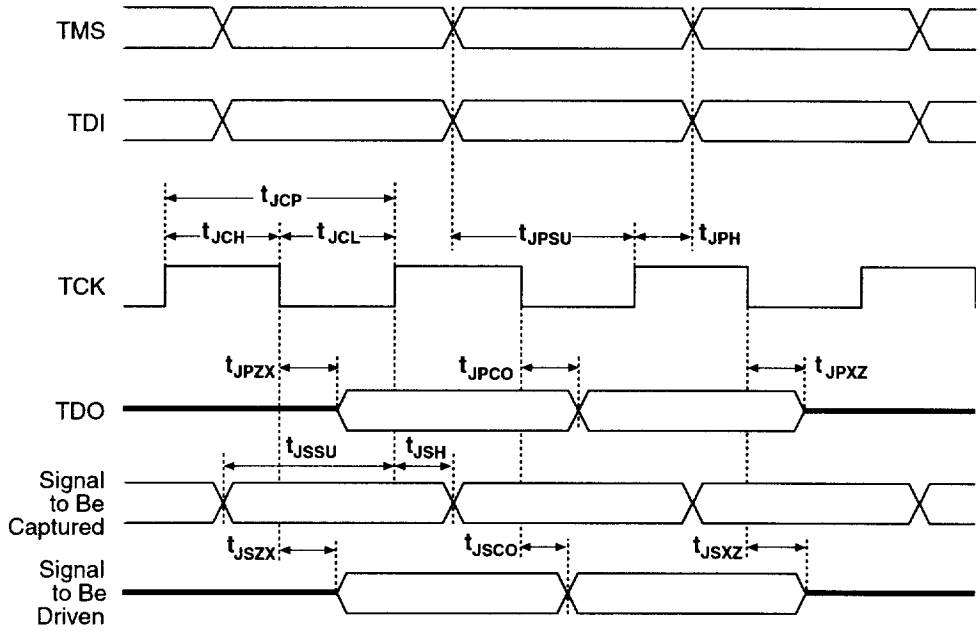


Table 22 shows the JTAG timing parameters and values for APEX 20K devices.

Table 22. APEX 20K JTAG Timing Parameters & Values

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		35	ns
t_{JSZX}	Update register high impedance to valid output		35	ns
t_{JSXZ}	Update register valid output to high impedance		35	ns

For more information, see the following documents:

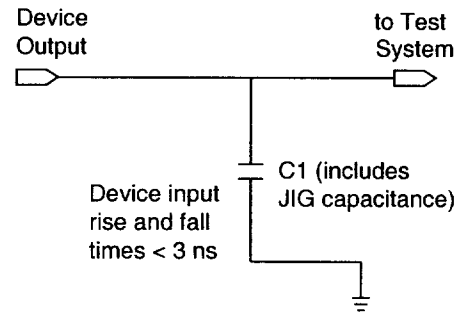
- *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *Jam Programming & Test Language Specification*

Generic Testing

Each APEX 20K device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for FLEX 10KE devices are made under conditions equivalent to those shown in Figure 32. Multiple test patterns can be used to configure devices during all stages of the production flow.

Figure 32. APEX 20K AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.



Operating Conditions

Tables 23 through 26 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 2.5-V APEX 20K devices.

Table 23. APEX 20K Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage	With respect to ground *(2)*	–0.5	3.6	V
V_{CCIO}			–0.5	4.6	V
V_I	DC input voltage		–0.5	4.6	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	PQFP, RQFP, TQFP, and BGA packages, under bias		135	° C
		Ceramic PGA packages, under bias		150	° C

Table 24. APEX 20K Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3), (4)*	2.375 (2.375)	2.625 (2.625)	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(3), (4)*	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	*(3), (4)*	2.375 (2.375)	2.625 (2.625)	V
V_I	Input voltage	*(2), (5)*	–0.5	4.1	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Operating temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 25. APEX 20K Device DC Operating Conditions (Part 1 of 2) *Notes (6), (7)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level LVTTL, CMOS, or 3.3-V PCI input voltage		1.7, 0.5 × V_{CCIO} *(8)*		4.1	V
V_{IL}	Low-level LVTTL, CMOS, or 3.3-V PCI input voltage		–0.5		0.8, 0.3 × V_{CCIO} *(8)*	V
V_{OH}	3.3-V high-level LVTTL output voltage	I_{OH} = –12 mA DC, V_{CCIO} = 3.00 V (9)	2.4			V
	3.3-V high-level LVCMOS output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 3.00 V *(9)*	V_{CCIO} – 0.2			V
	3.3-V high-level PCI output voltage	I_{OH} = –0.5 mA DC, V_{CCIO} = 3.00 to 3.60 V *(9)*	0.9 × V_{CCIO}			V
	2.5-V high-level output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 2.30 V *(9)*	2.1			V
		I_{OH} = –1 mA DC, V_{CCIO} = 2.30 V *(9)*	2.0			V
		I_{OH} = –2 mA DC, V_{CCIO} = 2.30 V *(9)*	1.7			V

Table 25. APEX 20K Device DC Operating Conditions (Part 2 of 2) *Notes (6), (7)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	3.3-V low-level LVTTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 3.00 V *(10)*			0.4	V
	3.3-V low-level LVCMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V *(10)*			0.2	V
	3.3-V low-level PCI output voltage	I_{OL} = 1.5 mA DC, V_{CCIO} = 3.00 to 3.60 V *(10)*			0.1 × V_{CCIO}	V
	2.5-V low-level output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 2.30 V *(10)*			0.2	V
		I_{OL} = 1 mA DC, V_{CCIO} = 2.30 V *(10)*			0.4	V
		I_{OL} = 2 mA DC, V_{CCIO} = 2.30 V *(10)*			0.7	V
I_I	Input pin leakage current	V_I = 4.1 to –0.5 V	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	V_O = 4.1 to –0.5 V	–10		10	µA
I_{CC0}	V_{CC} supply current (standby) (All ESBs in power-down mode)	V_I = ground, no load, no toggling inputs, -1 speed grade		10		mA
		V_I = ground, no load, no toggling inputs, -2, -3 speed grades		5		mA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	V_{CCIO} = 3.0 V *(11)*	20		50	kΩ
		V_{CCIO} = 2.375 V *(11)*	30		80	kΩ

Table 26. APEX 20K Device Capacitance *Note (12)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet.*
(2) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 4.6 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.
(5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
(6) Typical values are for T_A = 25 °C, V_{CCINT} = 2.5 V, and V_{CCIO} = 2.5 V or 3.3 V.
(7) These values are specified under the APEX 20K device recommended operating conditions, shown in Table 24 on page 60.
(8) The APEX 20K input buffers are compatible with 2.5-V and 3.3-V (LVTTL and LVCMOS) signals. Additionally, the input buffers are 3.3-V PCI compliant when V_{CCIO} and V_{CCINT} meet the relationship shown in Figure 33 on page 68.
(9) The I_{OH} parameter refers to high-level TTL, PCI, or CMOS output current.
(10) The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(11) Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO}.
(12) Capacitance is sample-tested only.

Tables 27 through 30 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 5.0-V tolerant APEX 20K devices. These devices are identified by a "V" suffix following the speed grade in the ordering code (e.g., EP20K400BC652-1V).

Table 27. APEX 20K 5.0-V Tolerant Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage	With respect to ground *(2)*	–0.5	3.6	V
V_{CCIO}			–0.5	4.6	V
V_I	DC input voltage		–2.0	5.75	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	PQFP, RQFP, TQFP, and BGA packages, under bias		135	° C
		Ceramic PGA packages, under bias		150	° C

Table 28. APEX 20K 5.0-V Tolerant Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3), (4)*	2.375 (2.375)	2.625 (2.625)	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(3), (4)*	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	*(3), (4)*	2.375 (2.375)	2.625 (2.625)	V
V_I	Input voltage	*(2), (5)*	–0.5	5.75	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Operating temperature	For commercial use	0	85	° C
		For industrial use	40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 29. APEX 20K 5.0-V Tolerant Device DC Operating Conditions (Part 1 of 2) *Notes (6), (7)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		1.7, 0.5 × V_{CCIO} *(8)*		5.75	V
V_{IL}	Low-level input voltage		–0.5		0.8, 0.3 × V_{CCIO} *(8)*	V
V_{OH}	3.3-V high-level TTL output voltage	I_{OH} = –8 mA DC, V_{CCIO} = 3.00 V *(9)*	2.4			V
	3.3-V high-level CMOS output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 3.00 V *(9)*	V_{CCIO} – 0.2			V
	3.3-V high-level PCI output voltage	I_{OH} = –0.5 mA DC, V_{CCIO} = 3.00 to 3.60 V *(9)*	0.9 × V_{CCIO}			V
	2.5-V high-level output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 2.30 V *(9)*	2.1			V
		I_{OH} = –1 mA DC, V_{CCIO} = 2.30 V *(9)*	2.0			V
		I_{OH} = –2 mA DC, V_{CCIO} = 2.30 V *(9)*	1.7			V

Table 29. APEX 20K 5.0-V Tolerant Device DC Operating Conditions (Part 2 of 2) *Notes (6), (7)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	3.3-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 3.00 V *(10)*			0.45	V
	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V *(10)*			0.2	V
	3.3-V low-level PCI output voltage	I_{OL} = 1.5 mA DC, V_{CCIO} = 3.00 to 3.60 V *(10)*			0.1 × V_{CCIO}	V
	2.5-V low-level output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 2.30 V *(10)*			0.2	V
		I_{OL} = 1 mA DC, V_{CCIO} = 2.30 V *(10)*			0.4	V
		I_{OL} = 2 mA DC, V_{CCIO} = 2.30 V *(10)*			0.7	V
I_I	Input pin leakage current	V_I = 5.75 to –0.5 V	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	V_O = 5.75 to –0.5 V	–10		10	µA
I_{CC0}	V_{CC} supply current (standby) (All ESBs in power-down mode)	V_I = ground, no load, no toggling inputs, -1 speed grade		10		mA
		V_I = ground, no load, no toggling inputs, -2, -3 speed grades		5		mA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	V_{CCIO} = 3.0 V 9 *(11)*	20		50	kΩ
		V_{CCIO} = 2.375 V *(11)*	30		80	kΩ

Table 30. APEX 20K 5.0-V Tolerant Device Capacitance *Note (12)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet.*

(2) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –0.5 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns.

(3) Numbers in parentheses are for industrial-temperature-range devices.

(4) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.

(5) All pins, including dedicated inputs, clock I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.

(6) Typical values are for T_A = 25 °C, V_{CCINT} = 2.5 V, and V_{CCIO} = 2.5 or 3.3 V.

(7) These values are specified in the APEX 20K device recommended operating conditions, shown in Table 26 on page 62.

(8) The APEX 20K input buffers are compatible with 2.5-V and 3.3-V (LVTTL and LVCMOS) signals. Additionally, the input buffers are 3.3-V PCI compliant when V_{CCIO} and V_{CCINT} meet the relationship shown in Figure 33 on page 68.

(9) The I_{OH} parameter refers to high-level TTL, PCI or CMOS output current.
(10) The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(11) Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO}.
(12) Capacitance is sample-tested only.

Tables 31 through 34 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 1.8-V APEX 20KE devices.

Table 31. APEX 20KE Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage	With respect to ground *(2)*	–0.5	2.5	V
V_{CCIO}			–0.5	4.6	V
V_I	DC input voltage		–0.5	4.6	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	°C
T_{AMB}	Ambient temperature	Under bias	–65	135	°C
T_J	Junction temperature	PQFP, RQFP, TQFP, and BGA packages, under bias		135	°C
		Ceramic PGA packages, under bias		150	°C

Table 32. APEX 20KE Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3), (4)*	1.71 (1.71)	1.89 (1.89)	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(3), (4)*	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	*(3), (4)*	2.375 (2.375)	2.625 (2.625)	V
V_I	Input voltage	*(2), (5)*	–0.5	4.1	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Operating temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 33. APEX 20KE Device DC Operating Conditions *Notes (6), (7)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level LVTTL, CMOS, or 3.3-V PCI input voltage		1.7, 0.5 × V_{CCIO} *(8)*		4.1	V
V_{IL}	Low-level LVTTL, CMOS, or 3.3-V PCI input voltage		–0.5		0.8, 0.3 × V_{CCIO} *(8)*	V
V_{OH}	3.3-V high-level LVTTL output voltage	I_{OH} = –12 mA DC, V_{CCIO} = 3.00 V *(9)*	2.4			V
	3.3-V high-level LVCMOS output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 3.00 V *(9)*	V_{CCIO} – 0.2			V
	3.3-V high-level PCI output voltage	I_{OH} = –0.5 mA DC, V_{CCIO} = 3.00 to 3.60 V *(9)*	0.9 × V_{CCIO}			V
	2.5-V high-level output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 2.30 V *(9)*	2.1			V
		I_{OH} = –1 mA DC, V_{CCIO} = 2.30 V *(9)*	2.0			V
		I_{OH} = –2 mA DC, V_{CCIO} = 2.30 V *(9)*	1.7			V
V_{OL}	3.3-V low-level LVTTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 3.00 V *(10)*			0.4	V
	3.3-V low-level LVCMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V *(10)*			0.2	V
	3.3-V low-level PCI output voltage	I_{OL} = 1.5 mA DC, V_{CCIO} = 3.00 to 3.60 V *(10)*			0.1 × V_{CCIO}	V
	2.5-V low-level output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 2.30 V *(10)*			0.2	V
		I_{OL} = 1 mA DC, V_{CCIO} = 2.30 V *(10)*			0.4	V
		I_{OL} = 2 mA DC, V_{CCIO} = 2.30 V *(10)*			0.7	V
I_I	Input pin leakage current	V_I = 4.1 to –0.5 V	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	V_O = 4.1 to –0.5 V	–10		10	µA
I_{CC0}	V_{CC} supply current (standby) (All ESBs in power-down mode)	V_I = ground, no load, no toggling inputs, -1 speed grade		10		mA
		V_I = ground, no load, no toggling inputs, -2, -3 speed grades		5		mA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	V_{CCIO} = 3.0 V *(11)*	20		50	kΩ
		V_{CCIO} = 2.375 V *(11)*	30		80	kΩ
		V_{CCIO} = 1.71 V *(11)*	60		150	kΩ

☞ For DC Operating Specifications on APEX 20KE I/O standards, please refer to *Application Note 117 (Using Selectable I/O Standards in Altera Devices).*

Table 34. APEX 20KE Device Capacitance *Note (12)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

Notes to tables:

(1) See the Operating Requirements for Altera Devices Data Sheet.
(2) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –0.5 V or overshoot to 4.6 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.
(5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
(6) Typical values are for T_A = 25° C, V_{CCINT} = 1.8 V, and V_{CCIO} = 1.8 V, 2.5 V or 3.3 V.
(7) These values are specified under the APEX 20KE device recommended operating conditions, shown in Table 32 on page 65.
(8) The APEX 20KE input buffers are compatible with 1.8-V, 2.5-V and 3.3-V (LVTTL and LVCMOS) signals. Additionally, the input buffers are 3.3-V PCI compliant. Input buffers also meet specifications for GTL+, CTT, AGP, SSTL-2, SSTL-3, and HSTL.
(9) The I_{OH} parameter refers to high-level TTL, PCI, or CMOS output current.
(10) The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(11) Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO}.
(12) Capacitance is sample-tested only.

Figure 33 shows the relationship between V_{CCIO} and V_{CCINT} for 3.3-V PCI compliance on APEX 20K devices. For information on this relationship on APEX 20KE devices, contact Altera Applications.

Figure 33. Relationship between V_{CCIO} & V_{CCINT} for 3.3-V PCI Compliance

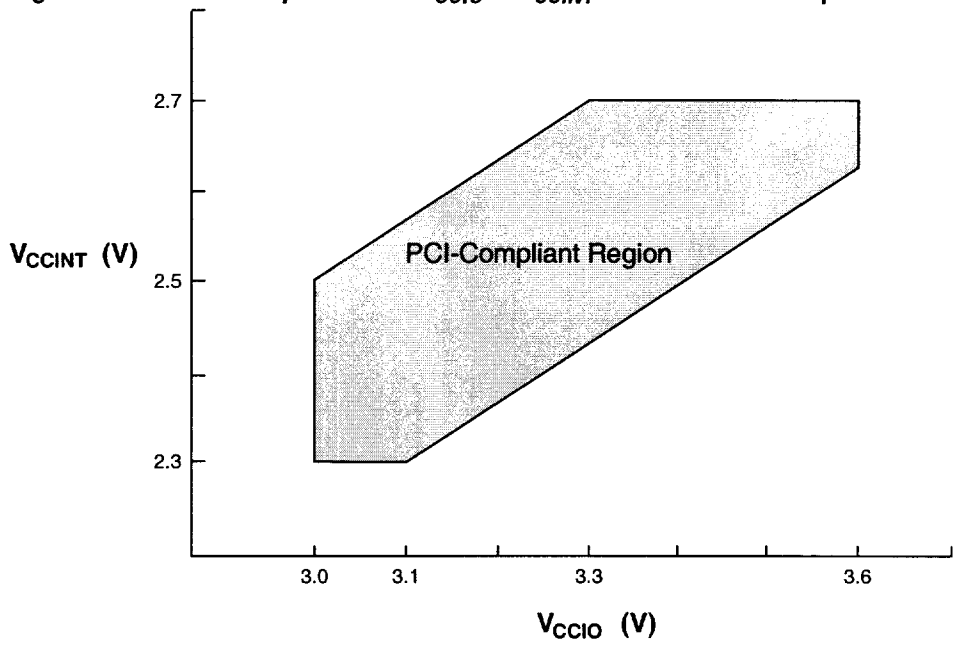


Figure 34 shows the typical output drive characteristics of APEX 20K devices with 3.3-V and 2.5-V V_{CCIO}. The output driver is compatible with the 3.3-V *PCI Local Bus Specification, Revision 2.2* (when VCCIO pins are connected to 3.3 V). 5-V tolerant APEX 20K devices in the -1 speed grade are 5-V PCI compliant over all operating conditions.

Figure 34. Output Drive Characteristics of APEX 20K Device

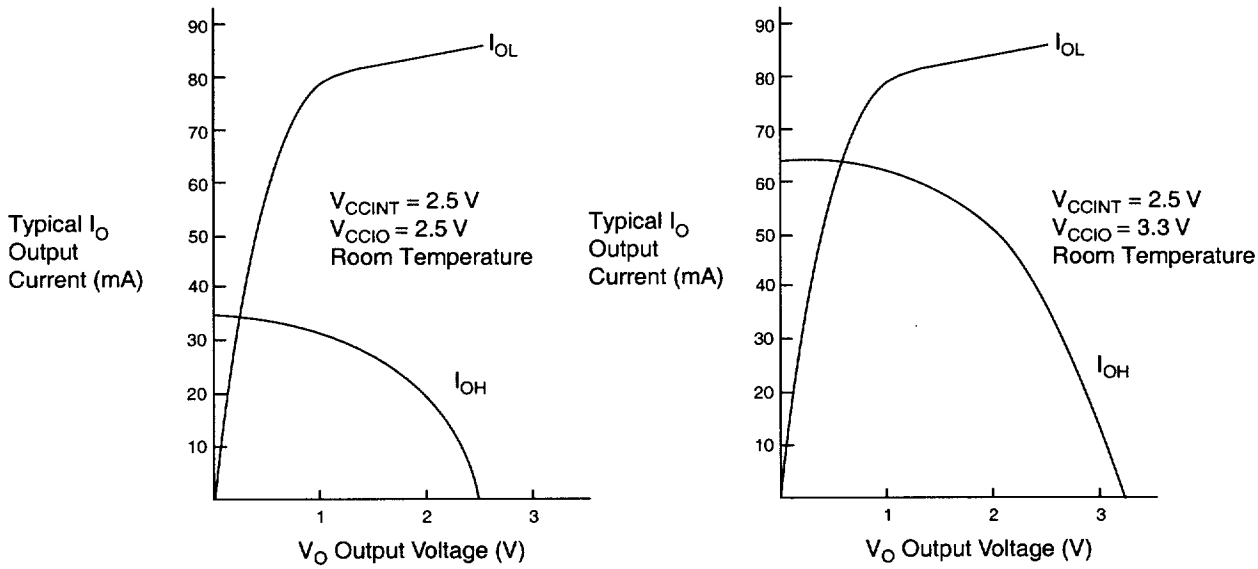
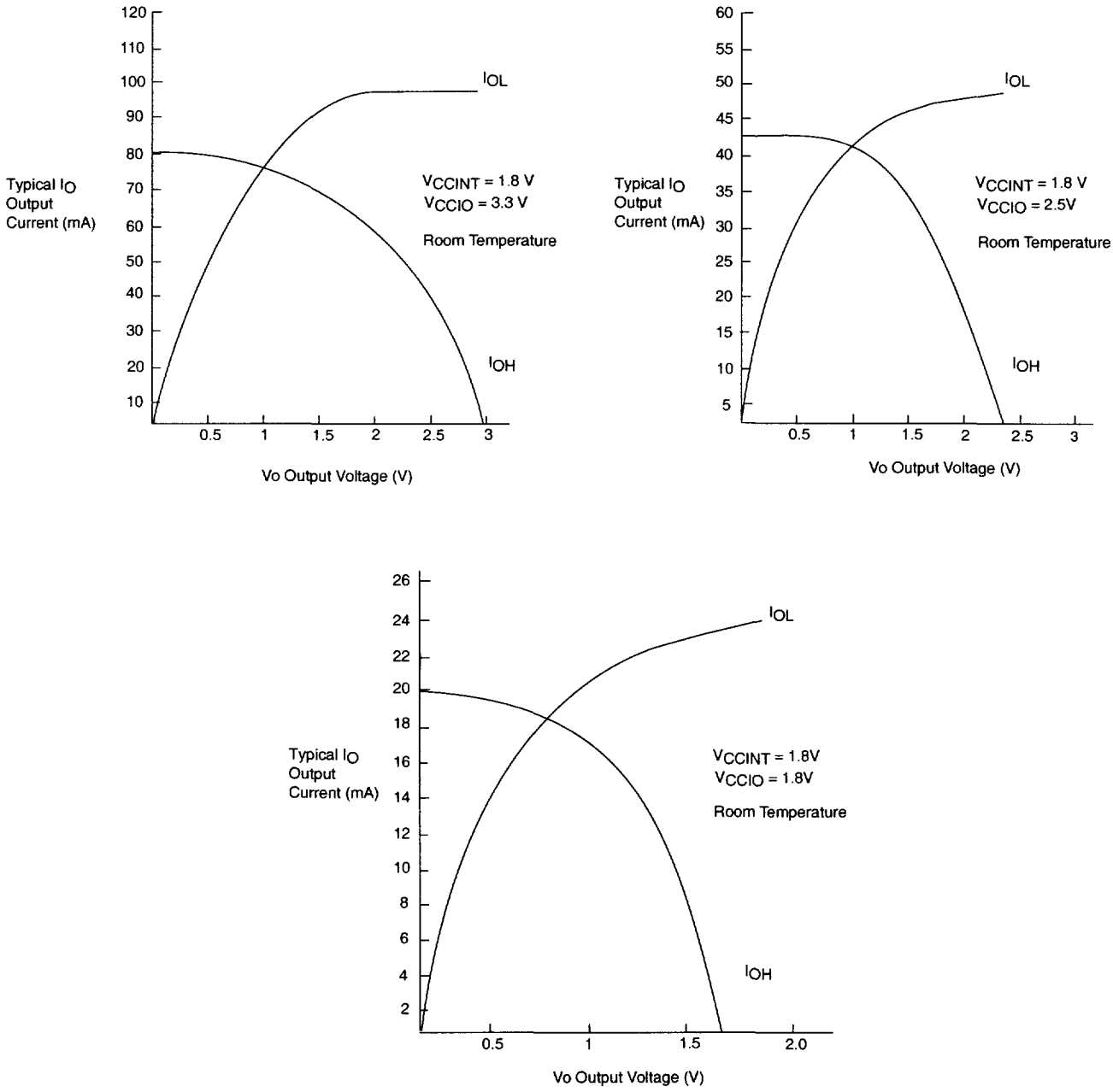


Figure 35 shows the output drive characteristics of APEX 20KE devices.

Figure 35. Output Drive Characteristics of APEX 20KE Devices

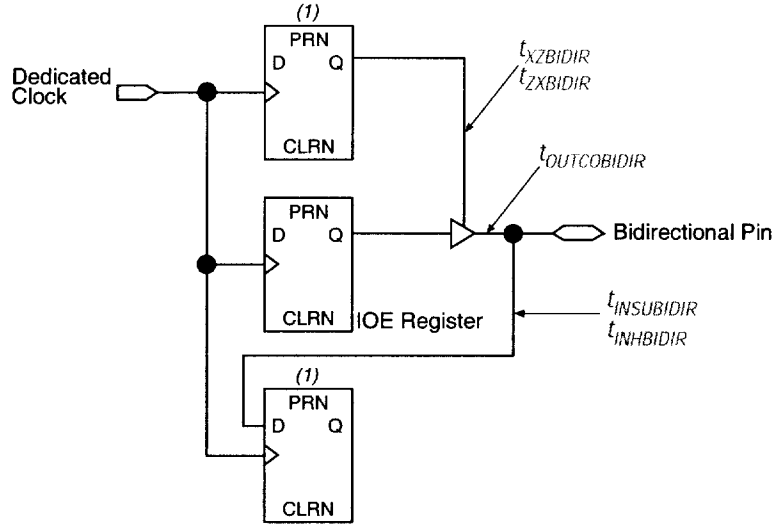


Timing Model

The continuous, high-performance FastTrack and MegaLAB interconnect routing resources ensure predictable performance, accurate simulation, and accurate timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

Figure 36 shows the timing model for bidirectional I/O pin timing.

Figure 36. Synchronous Bidirectional Pin External Timing



Note:

(1) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin.

Tables 35 and 36 describe APEX 20K external timing parameters.

Table 35. APEX 20K External Timing Parameters *Note (1)*

Symbol	Clock Parameter	Conditions
t_{INSU}	Setup time with global clock at IOE register	
t_{INH}	Hold time with global clock at IOE register	
t_{OUTCO}	Clock-to-output delay with global clock at IOE register	
t_{PCISU}	Setup time with global clock for registers used in PCI designs	
t_{PCICO}	Clock-to-output delay with global clock for registers used in PCI designs	
t_{PCIH}	Hold time with global clock for registers used in PCI designs	

Table 36. External Bidirectional Timing Parameters Note (1)		
Symbol	**Parameter**	**Condition**
$t_{INSUBIDIR}$	Setup time for bidirectional pins with global clock at same-row or same-column LE register	
$t_{INHBIDIR}$	Hold time for bidirectional pins with global clock at same-row or same-column LE register	
$t_{OUTCOBIDIR}$	Clock-to-output delay for bidirectional pins with global clock at IOE register	C1 = 35 pF
$t_{XZBIDIR}$	Synchronous IOE output buffer disable delay	C1 = 35 pF
$t_{ZXBIDIR}$	Synchronous IOE output buffer enable delay, slow slew rate = off	C1 = 35 pF

Note to tables:
(1) These timing parameters are sample-tested only.

Figure 37 shows the f_{MAX} timing model for APEX 20K and APEX 20KE devices.

Figure 37. f_{MAX} Timing Model

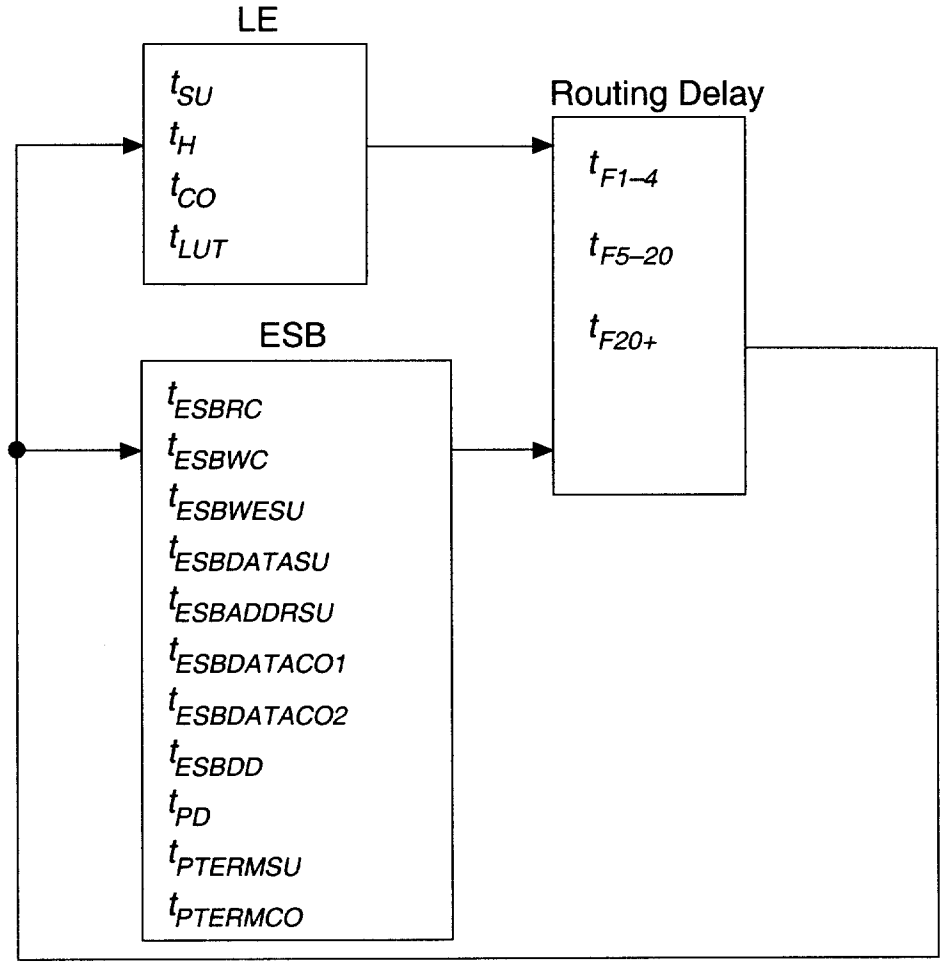


Table 37describes the f_{MAX} timing parameters shown in Figure 37.

Table 37. APEX 20K & APEX 20KE f_{MAX} Timing Parameters

Symbol	Parameter
t_{SU}	LE register setup time before clock
t_{H}	LE register hold time before clock
t_{CO}	LE register clock-to-output delay
t_{LUT}	LUT delay for data-in
t_{ESBRC}	ESB Asynchronous read cycle time
t_{ESBWC}	ESB Asynchronous write cycle time
$t_{ESBWESU}$	ESB WE setup time before clock when using input register
$t_{ESBDATASU}$	ESB data setup time before clock when using input register
$t_{ESBADDRSU}$	ESB address setup time before clock when using input registers
$t_{ESBDATACO1}$	ESB clock-to-output delay when using output registers
$t_{ESBDATACO2}$	ESB clock-to-output delay without output registers
t_{ESBDD}	ESB data-in to data-out delay for RAM mode
t_{PD}	ESB macrocell input to non-registered output
$t_{PTERMSU}$	ESB macrocell register setup time before clock
$t_{PTERMCO}$	ESB macrocell register clock-to-output delay
t_{F1-4}	Fanout delay using local interconnect
t_{F5-20}	Fanout delay using MegaLab Interconnect
t_{F20+}	Fanout delay using FastTrack Interconnect
t_{CH}	Minimum clock high time from clock pin
t_{CL}	Minimum clock low time from clock pin
t_{CLRP}	LE clear pulse width
t_{PREP}	LE preset pulse width
t_{ESBCH}	Clock high time
t_{ESBCL}	Clock low time
t_{ESBWP}	Write pulse width
t_{ESBRP}	Read pulse width

Tables 38 through 43 show the f_{MAX} timing parameters for EP20K100, EP20K200, EP20K400, EP20K300E, EP20K400E, EP20K600E, and EP20K1000E devices.

Table 38. EP20K100 f_{MAX} Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade	
	Min	Max	Min	Max	Min	Max
t_{SU}	0.5		0.6		0.8	
t_{H}	0.7		0.8		1.0	
t_{CO}		0.3		0.4		0.5
t_{LUT}		0.8		1.0		1.3
t_{ESBRC}		1.7		2.1		2.4
t_{ESBWC}		5.7		6.9		8.1
$t_{ESBWESU}$	3.3		3.9		4.6	
$t_{ESBDATASU}$	2.2		2.7		3.1	
$t_{ESBADDRSU}$	2.4		2.9		3.3	
$t_{ESBDATACO1}$		1.3		1.6		1.8
$t_{ESBDATACO2}$		2.6		3.1		3.6
t_{ESBDD}		2.5		3.3		3.6
t_{PD}		2.5		3.0		3.6
$t_{PTERMSU}$	2.3		2.6		3.2	
$t_{PTERMCO}$		1.5		1.8		2.1
t_{F1-4}		0.5		0.6		0.7
t_{F5-20}		1.6		1.7		1.8
t_{F20+}		2.2		2.2		2.3
t_{CH}	2.0		2.5		3.0	
t_{CL}	2.0		2.5		3.0	
t_{CLRP}	0.3		0.4		0.4	
t_{PREP}	0.5		0.5		0.5	
t_{ESBCH}	2.0		2.5		3.0	
t_{ESBCL}	2.0		2.5		3.0	
t_{ESBWP}	1.6		1.9		2.2	
t_{ESBRP}	1.0		1.3		1.4	

Table 39. EP20K200 f_{MAX} Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade	
	Min	Max	Min	Max	Min	Max
t_{SU}	0.5		0.6		0.8	
t_{H}	0.7		0.8		1.0	
t_{CO}		0.3		0.4		0.5
t_{LUT}		0.8		1.0		1.3
t_{ESBRC}		1.7		2.1		2.4
t_{ESBWC}		5.7		6.9		8.1
$t_{ESBWESU}$	3.3		3.9		4.6	
$t_{ESBDATASU}$	2.2		2.7		3.1	
$t_{ESBADDRSU}$	2.4		2.9		3.3	
$t_{ESBDATACO1}$		1.3		1.6		1.8
$t_{ESBDATACO2}$		2.6		3.1		3.6
t_{ESBDD}		2.5		3.3		3.6
t_{PD}		2.5		3.0		3.6
$t_{PTERMSU}$	2.3		2.7		3.2	
$t_{PTERMCO}$		1.5		1.8		2.1
t_{F1-4}		0.5		0.6		0.7
t_{F5-20}		1.6		1.7		1.8
t_{F20+}		2.2		2.2		2.3
t_{CH}	2.0		2.5		3.0	
t_{CL}	2.0		2.5		3.0	
t_{CLRP}	0.3		0.4		0.4	
t_{PREP}	0.4		0.5		0.5	
t_{ESBCH}	2.0		2.5		3.0	
t_{ESBCL}	2.0		2.5		3.0	
t_{ESBWP}	1.6		1.9		2.2	
t_{ESBRP}	1.0		1.3		1.4	

Table 40. EP20K400 f_{MAX} Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade	
	Min	Max	Min	Max	Min	Max
t_{SU}	0.1		0.3		0.6	
t_{H}	0.5		0.8		0.9	
t_{CO}		0.1		0.4		0.6
t_{LUT}		1.0		1.2		1.4
t_{ESBRC}		1.7		2.1		2.4
t_{ESBWC}		5.7		6.9		8.1
$t_{ESBWESU}$	3.3		3.9		4.6	
$t_{ESBDATASU}$	2.2		2.7		3.1	
$t_{ESBADDRSU}$	2.4		2.9		3.3	
$t_{ESBDATACO1}$		1.3		1.6		1.8
$t_{ESBDATACO2}$		2.5		3.1		3.6
t_{ESBDD}		2.5		3.3		3.6
t_{PD}		2.5		3.1		3.6
$t_{PTERMSU}$	1.7		2.1		2.4	
$t_{PTERMCO}$		1.0		1.2		1.4
t_{F1-4}		0.4		0.5		0.6
t_{F5-20}		2.6		2.8		2.9
t_{F20+}		3.7		3.8		3.9
t_{CH}	2.0		2.5		3.0	
t_{CL}	2.0		2.5		3.0	
t_{CLRP}	0.5		0.6		0.8	
t_{PREP}	0.5		0.5		0.5	
t_{ESBCH}	2.0		2.5		3.0	
t_{ESBCL}	2.0		2.5		3.0	
t_{ESBWP}	1.5		1.9		2.2	
t_{ESBRP}	1.0		1.2		1.4	

Table 41. EP20K300E f_{MAX} Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade	
	Min	Max	Min	Max	Min	Max
t_{SU}	0.1		0.3		0.6	
t_{H}	0.3		0.7		0.9	
t_{CO}		0.1		0.4		0.6
t_{LUT}		0.9		1.0		1.2
t_{ESBRC}		1.5		1.8		2.2
t_{ESBWC}		5.2		5.9		7.4
$t_{ESBWESU}$	2.9		3.3		4.2	
$t_{ESBDATASU}$	1.9		2.2		2.9	
$t_{ESBADDRSU}$	2.2		2.4		3.0	
$t_{ESBDATACO1}$		1.3		1.4		1.7
$t_{ESBDATACO2}$		2.3		2.6		3.3
t_{ESBDD}		2.3		3.2		3.5
t_{PD}		2.3		2.6		3.3
$t_{PTERMSU}$	1.6		1.8		2.2	
$t_{PTERMCO}$		0.9		1.1		1.3
t_{F1-4}		0.3		0.4		0.5
t_{F5-20}		2.6		2.6		2.6
t_{F20+}		3.5		3.6		3.6
t_{CH}	2.0		2.2		2.8	
t_{CL}	2.0		2.2		2.8	
t_{CLRP}	0.5		0.6		0.7	
t_{PREP}	0.5		0.5		0.5	
t_{ESBCH}	2.0		2.2		2.8	
t_{ESBCL}	2.0		2.2		2.8	
t_{ESBWP}	1.4		1.6		2.0	
t_{ESBRP}	0.9		1.0		1.3	

Table 42. EP20K400E f_{MAX} Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade	
	Min	Max	Min	Max	Min	Max
t_{SU}	0.1		0.3		0.6	
t_{H}	0.3		0.7		0.9	
t_{CO}		0.1		0.4		0.6
t_{LUT}		0.8		0.9		1.1
t_{ESBRC}		1.5		1.8		2.2
t_{ESBWC}		5.2		5.9		7.4
$t_{ESBWESU}$	2.9		3.3		4.2	
$t_{ESBDATASU}$	1.9		2.2		2.9	
$t_{ESBADDRSU}$	2.2		2.4		3.0	
$t_{ESBDATACO1}$		1.3		1.4		1.7
$t_{ESBDATACO2}$		2.3		2.6		3.3
t_{ESBDD}		2.3		3.2		3.5
t_{PD}		2.3		2.6		3.3
$t_{PTERMSU}$	1.6		1.8		2.2	
$t_{PTERMCO}$		0.9		1.1		1.3
t_{F1-4}		0.3		0.4		0.5
t_{F5-20}		2.6		2.6		2.6
t_{F20+}		3.5		3.6		3.6
t_{CH}	2.0		2.2		2.8	
t_{CL}	2.0		2.2		2.8	
t_{CLRP}	0.5		0.6		0.7	
t_{PREP}	0.5		0.5		0.5	
t_{ESBCH}	2.0		2.2		2.8	
t_{ESBCL}	2.0		2.2		2.8	
t_{ESBWP}	1.4		1.6		2.0	
t_{ESBRP}	0.9		1.0		1.3	

Table 43. EP20K600E f_{MAX} Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade	
	Min	Max	Min	Max	Min	Max
t_{SU}	0.1		0.3		0.6	
t_{H}	0.5		0.7		0.9	
t_{CO}		0.1		0.4		0.6
t_{LUT}		0.8		1.1		1.3
t_{ESBRC}		1.5		1.8		2.2
t_{ESBWC}		5.2		5.9		7.4
$t_{ESBWESU}$	2.9		3.3		4.2	
$t_{ESBDATASU}$	1.9		2.2		2.9	
$t_{ESBADDRSU}$	2.2		2.4		3.0	
$t_{ESBDATACO1}$		1.3		1.4		1.7
$t_{ESBDATACO2}$		2.3		2.6		3.3
t_{ESBDD}		2.4		3.2		3.5
t_{PD}		2.3		2.6		3.3
$t_{PTERMSU}$	1.6		1.8		2.2	
$t_{PTERMCO}$		0.9		1.1		1.3
t_{F1-4}		0.3		0.4		0.5
t_{F5-20}		2.6		2.6		2.7
t_{F20+}		3.5		3.6		3.7
t_{CH}	2.0		2.2		2.8	
t_{CL}	2.0		2.2		2.8	
t_{CLRP}	0.5		0.6		0.7	
t_{PREP}	0.5		0.5		0.5	
t_{ESBCH}	2.0		2.2		2.8	
t_{ESBCL}	2.0		2.2		2.8	
t_{ESBWP}	1.4		1.6		2.0	
t_{ESBRP}	0.9		1.0		1.3	

Table 44. EP20K1000E f_{MAX} Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade	
	Min	Max	Min	Max	Min	Max
t_{SU}	0.1		0.3		0.6	
t_{H}	0.5		0.7		0.9	
t_{CO}		0.1		0.4		0.6
t_{LUT}		0.9		1.1		1.3
t_{ESBRC}		1.5		1.8		2.2
t_{ESBWC}		5.2		5.9		7.4
$t_{ESBWESU}$	2.9		3.3		4.2	
$t_{ESBDATASU}$	1.9		2.2		2.9	
$t_{ESBADDRSU}$	2.2		2.4		3.0	
$t_{ESBDATACO1}$		1.3		1.4		1.7
$t_{ESBDATACO2}$		2.3		2.6		3.3
t_{ESBDD}		2.4		3.2		3.5
t_{PD}		2.3		2.6		3.3
$t_{PTERMSU}$	1.6		1.8		2.2	
$t_{PTERMCO}$		0.9		1.1		1.3
t_{F1-4}		0.3		0.4		0.5
t_{F5-20}		4.6		4.6		4.8
t_{F20+}		4.1		4.2		4.4
t_{CH}	2.0		2.2		2.8	
t_{CL}	2.0		2.2		2.8	
t_{CLRP}	0.5		0.6		0.7	
t_{PREP}	0.5		0.5		0.5	
t_{ESBCH}	2.0		2.2		2.8	
t_{ESBCL}	2.0		2.2		2.8	
t_{ESBWP}	1.4		1.6		2.0	
t_{ESBRP}	0.9		1.0		1.3	

Tables 45 through 62 show the I/O external and external bidirectional timing parameter values for APEX 20K and APEX 20KE devices.

Table 45. EP20K100 External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU} (1)	2.3		2.8		3.2		ns
t_{INH} (1)	0.0		0.0		0.0		ns
t_{OUTCO} (1)	2.0	4.5	2.0	4.9	2.0	6.6	ns
t_{INSU} (2)	1.1		1.2		–		ns
t_{INH} (2)	0.0		0.0		–		ns
t_{OUTCO} (2)	0.5	2.7	0.5	3.1	–	4.8	ns

Table 46. EP20K100 External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ (1)	2.3		2.8		3.2		ns
$t_{INHBIDIR}$ (1)	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ (1)	2.0	4.5	2.0	4.9	2.0	6.6	ns
$t_{XZBIDIR}$ (1)		5.0		5.9		6.9	ns
$t_{ZXBIDIR}$ (1)		5.0		5.9		6.9	ns
$t_{INSUBIDIR}$ (2)	1.0		1.2		–		ns
$t_{INHBIDIR}$ (2)	0.0		0.0		–		ns
$t_{OUTCOBIDIR}$ (2)	0.5	2.7	0.5	3.1	–	–	ns
$t_{XZBIDIR}$ (2)		4.3		5.0		–	ns
$t_{ZXBIDIR}$ (2)		4.3		5.0		–	ns

Notes to tables:

(1) This parameter is measured without using ClockLock or ClockBoost circuits.

(2) This parameter is measured using ClockLock or ClockBoost circuits.

Table 47. EP20K100E External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU} (1)	2.2		2.3		2.4		ns
t_{INH} (1)	0.0		0.0		0.0		ns
t_{OUTCO} (1)	2.0	4.9	2.0	5.3	2.0	5.8	ns
t_{INSU} (2)	1.6		1.7		–		ns
t_{INH} (2)	0.0		0.0		–		ns
t_{OUTCO} (2)	0.5	3.0	0.5	3.3	–	–	ns

Table 48. EP20K100E External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ (1)	2.2		2.3		2.4		ns
$t_{INHBIDIR}$ (1)	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ (1)	2.0	4.9	2.0	5.3	2.0	5.8	ns
$t_{XZBIDIR}$ (1)		5.7		6.8		8.3	ns
$t_{ZXBIDIR}$ (1)		5.7		6.8		8.3	ns
$t_{INSUBIDIR}$ (2)	1.8		2.5		–		ns
$t_{INHBIDIR}$ (2)	0.0		0.0		–		ns
$t_{OUTCOBIDIR}$ (2)	0.5	3.0	0.5	3.3	–	–	ns
$t_{XZBIDIR}$ (2)		3.7		4.3		–	ns
$t_{ZXBIDIR}$ (2)		3.7		4.3		–	ns

Notes to tables:

(1) This parameter is measured without using ClockLock or ClockBoost circuits.

(2) This parameter is measured using ClockLock or ClockBoost circuits.

Table 49. EP20K200 External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU} (1)	1.9		2.3		2.6		ns
t_{INH} (1)	0.0		0.0		0.0		ns
t_{OUTCO} (1)	2.0	4.6	2.0	5.6	2.0	6.8	ns
t_{INSU} (2)	1.1		1.2		–		ns
t_{INH} (2)	0.0		0.0		–		ns
t_{OUTCO} (2)	0.5	2.7	0.5	3.1	–	–	ns

Table 50. EP20K200 External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ (1)	1.9		2.3		2.6		ns
$t_{INHBIDIR}$ (1)	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ (1)	2.0	4.6	2.0	5.6	2.0	6.8	ns
$t_{XZBIDIR}$ (1)		5.0		5.9		6.9	ns
$t_{ZXBIDIR}$ (1)		5.0		5.9		6.9	ns
$t_{INSUBIDIR}$ (2)	1.1		1.2		–		ns
$t_{INHBIDIR}$ (2)	0.0		0.0		–		ns
$t_{OUTCOBIDIR}$ (2)	0.5	2.7	0.5	3.1	–	–	ns
$t_{XZBIDIR}$ (2)		4.3		5.0		–	ns
$t_{ZXBIDIR}$ (2)		4.3		5.0		–	ns

Notes to tables:

(1) This parameter is measured without using ClockLock or ClockBoost circuits.

(2) This parameter is measured using ClockLock or ClockBoost circuits.

Table 51. EP20K200E External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU} (1)	2.3		2.4		2.5		ns
t_{INH} (1)	0.0		0.0		0.0		ns
t_{OUTCO} (1)	2.0	5.1	2.0	5.6	2.0	6.1	ns
t_{INSU} (2)	1.9		2.0		–		ns
t_{INH} (2)	0.0		0.0		–		ns
t_{OUTCO} (2)	0.5	3.0	0.5	3.3	–	–	ns

Table 52. EP20K200E External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ (1)	2.3		2.4		2.5		ns
$t_{INHBIDIR}$ (1)	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ (1)	2.0	5.1	2.0	5.6	2.0	6.1	ns
$t_{XZBIDIR}$ (1)		6.0		7.3		9.2	ns
$t_{ZXBIDIR}$ (1)		6.0		7.3		9.2	ns
$t_{INSUBIDIR}$ (2)	1.8		2.0		–		ns
$t_{INHBIDIR}$ (2)	0.0		0.0		–		ns
$t_{OUTCOBIDIR}$ (2)	0.5	3.0	0.5	3.3	–	–	ns
$t_{XZBIDIR}$ (2)		4.1		4.5		–	ns
$t_{ZXBIDIR}$ (2)		4.1		4.5		–	ns

Notes to tables:

(1) This parameter is measured without using ClockLock or ClockBoost circuits.

(2) This parameter is measured using ClockLock or ClockBoost circuits.

Table 53. EP20K300E External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU} (1)	2.3		2.4		2.5		ns
t_{INH} (1)	0.0		0.0		0.0		ns
t_{OUTCO} (1)	2.0	5.2	2.0	5.7	2.0	6.2	ns
t_{INSU} (2)	1.8		1.9		–		ns
t_{INH} (2)	0.0		0.0		–		ns
t_{OUTCO} (2)	0.5	2.8	0.5	3.0	–	–	ns

Table 54. EP20K300E External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ (1)	2.3		2.4		2.5		ns
$t_{INHBIDIR}$ (1)	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ (1)	2.0	5.2	2.0	5.7	2.0	6.2	ns
$t_{XZBIDIR}$ (1)		6.0		7.2		9.2	ns
$t_{ZXBIDIR}$ (1)		6.0		7.2		9.2	ns
$t_{INSUBIDIR}$ (2)	1.8		1.9		–		ns
$t_{INHBIDIR}$ (2)	0.0		0.0		–		ns
$t_{OUTCOBIDIR}$ (2)	0.5	2.8	0.5	3.0	–	–	ns
$t_{XZBIDIR}$ (2)		3.3		4.1		–	ns
$t_{ZXBIDIR}$ (2)		3.3		4.1		–	ns

Notes to tables:

(1) This parameter is measured without using ClockLock or ClockBoost circuits.

(2) This parameter is measured using ClockLock or ClockBoost circuits.

Table 55. EP20K400 External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU} (1)	1.4		1.8		2.0		ns
t_{INH} (1)	0.0		0.0		0.0		ns
t_{OUTCO} (1)	2.0	4.9	2.0	6.1	2.0	7.0	ns
t_{INSU} (2)	0.4		1.0		–		ns
t_{INH} (2)	0.0		0.0		–		ns
t_{OUTCO} (2)	0.5	3.1	0.5	4.1	–	–	ns

Table 56. EP20K400 External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ (1)	1.4		1.8		2.0		ns
$t_{INHBIDIR}$ (1)	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ (1)	2.0	4.9	2.0	6.1	2.0	7.0	ns
$t_{XZBIDIR}$ (1)		7.3		8.9		10.3	ns
$t_{ZXBIDIR}$ (1)		7.3		8.9		10.3	ns
$t_{INSUBIDIR}$ (2)	0.5		1.0		–		ns
$t_{INHBIDIR}$ (2)	0.0		0.0		–		ns
$t_{OUTCOBIDIR}$ (2)	0.5	3.1	0.5	4.1	–	–	ns
$t_{XZBIDIR}$ (2)		6.2		7.6		–	ns
$t_{ZXBIDIR}$ (2)		6.2		7.6		–	ns

Notes to tables:

(1) This parameter is measured without using ClockLock or ClockBoost circuits.

(2) This parameter is measured using ClockLock or ClockBoost circuits.

Table 57. EP20K400E External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU} (1)	2.5		2.6		2.8		ns
t_{INH} (1)	0.0		0.0		0.0		ns
t_{OUTCO} (1)	2.0	5.3	2.0	5.8	2.0	6.3	ns
t_{INSU} (2)	3.2		3.4		–		ns
t_{INH} (2)	0.0		0.0		–		ns
t_{OUTCO} (2)	0.5	2.2	0.5	2.4	–	–	ns

Table 58. EP20K400E External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ (1)	2.5		2.6		2.8		ns
$t_{INHBIDIR}$ (1)	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ (1)	2.0	5.3	2.0	5.8	2.0	6.3	ns
$t_{XZBIDIR}$ (1)		5.4		6.0		7.0	ns
$t_{ZXBIDIR}$ (1)		5.4		6.0		7.0	ns
$t_{INSUBIDIR}$ (2)	3.2		3.4		–		ns
$t_{INHBIDIR}$ (2)	0.0		0.0		–		ns
$t_{OUTCOBIDIR}$ (2)	0.5	2.2	0.5	2.4	–	–	ns
$t_{XZBIDIR}$ (2)		3.5		4.0		–	ns
$t_{ZXBIDIR}$ (2)		3.5		4.0		–	ns

Notes to tables:

(1) This parameter is measured without using ClockLock or ClockBoost circuits.

(2) This parameter is measured using ClockLock or ClockBoost circuits.

Table 59. EP20K600E External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU} (1)	2.6		2.7		2.9		ns
t_{INH} (1)	0.0		0.0		0.0		ns
t_{OUTCO} (1)	2.0	5.5	2.0	6.0	2.0	6.6	ns
t_{INSU} (2)	1.9		2.0		–		ns
t_{INH} (2)	0.0		0.0		–		ns
t_{OUTCO} (2)	0.5	2.6	0.5	2.9	–	–	ns

Table 60. EP20K600E External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ (1)	2.6		2.7		2.9		ns
$t_{INHBIDIR}$ (1)	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ (1)	2.0	5.5	2.0	6.0	2.0	6.6	ns
$t_{XZBIDIR}$ (1)		6.3		7.6		9.7	ns
$t_{ZXBIDIR}$ (1)		6.3		7.6		9.7	ns
$t_{INSUBIDIR}$ (2)	1.9		2.0		–		ns
$t_{INHBIDIR}$ (2)	0.0		0.0		–		ns
$t_{OUTCOBIDIR}$ (2)	0.5	2.6	0.5	2.9	–	–	ns
$t_{XZBIDIR}$ (2)		3.3		4.1		–	ns
$t_{ZXBIDIR}$ (2)		3.3		4.1		–	ns

Notes to tables:

(1) This parameter is measured without using ClockLock or ClockBoost circuits.

(2) This parameter is measured using ClockLock or ClockBoost circuits.

Table 61. EP20K1000E External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU} (1)	2.7		2.8		3.0		ns
t_{INH} (1)	0.0		0.0		0.0		ns
t_{OUTCO} (1)	2.0	5.8	2.0	6.3	2.0	6.9	ns
t_{INSU} (2)	1.6		1.7		–		ns
t_{INH} (2)	0.0		0.0		–		ns
t_{OUTCO} (2)	0.5	2.3	0.5	2.5	–	–	ns

Table 62. EP20K1000E External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ (1)	2.7		2.8		3.0		ns
$t_{INHBIDIR}$ (1)	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ (1)	2.0	5.8	2.0	6.3	2.0	6.9	ns
$t_{XZBIDIR}$ (1)		6.6		7.9		9.7	ns
$t_{ZXBIDIR}$ (1)		6.6		7.9		9.7	ns
$t_{INSUBIDIR}$ (2)	3.8		5.2		–		ns
$t_{INHBIDIR}$ (2)	0.0		0.0		–		ns
$t_{OUTCOBIDIR}$ (2)	0.5	2.3	0.5	2.5	–	–	ns
$t_{XZBIDIR}$ (2)		3.3		4.1		–	ns
$t_{ZXBIDIR}$ (2)		3.3		4.1		–	ns

Notes to tables:

(1) This parameter is measured without using ClockLock or ClockBoost circuits.

(2) This parameter is measured using ClockLock or ClockBoost circuits. ClockShift was not used in this measurement. ClockShift can be used to adjust the setup and clock-to-output times to achieve the desired results.

Tables 63 and 64 show selectable I/O standard input and output delays for APEX 20KE devices. If you select an I/O standard input or output delay other than LVCMOS, add or subtract the selected speed grade to or from the LVCMOS value.

Table 63. Selectable I/O Standard Input Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min
LVCMOS		0.0		0.0		0.0	ns
LVTTL		0.0		0.0		0.0	ns
2.5 V		0.1		0.2		0.2	ns
1.8 V		0.5		0.6		0.8	ns
PCI		0.4		0.5		0.7	ns
GTL+		–0.3		–0.4		–0.5	ns
SSTL-3 Class I		–0.4		–0.5		–0.6	ns
SSTL-3 Class II		–0.4		–0.5		–0.6	ns
SSTL-2 Class I		–0.3		–0.3		–0.4	ns
SSTL-2 Class II		–0.3		–0.3		–0.4	ns
LVDS		–0.2		–0.3		–0.4	ns
CTT		–0.3		–0.3		–0.4	ns
AGP		0.0		0.1		0.1	ns

Table 64. Selectable I/O Standard Output Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min
LVCMOS		0.0		0.0		0.0	ns
LVTTL		0.0		0.0		0.0	ns
2.5 V		0.5		0.6		0.7	ns
1.8 V		1.7		2.2		2.7	ns
PCI		–0.2		–0.3		–0.4	ns
GTL+		–0.4		–0.5		–0.6	ns
SSTL-3 Class I		–0.1		–0.2		–0.2	ns
SSTL-3 Class II		–0.6		–0.8		–1.0	ns
SSTL-2 Class I		0.0		0.0		0.0	ns
SSTL-2 Class II		–0.4		–0.5		–0.6	ns
LVDS		–0.8		–1.0		–1.2	ns
CTT		–0.2		–0.3		–0.4	ns
AGP		–0.4		–0.5		–0.7	ns

Power Consumption

To estimate device power consumption, use the interactive power estimator on the Altera web site at **http://www.altera.com**.

Configuration & Operation

The APEX 20K architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

Operating Modes

The APEX architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

Before and during device configuration, all I/O pins are pulled to V_{CCIO} by a built-in weak pull-up resistor.

SRAM configuration elements allow APEX 20K devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. In-field upgrades can be performed by distributing new configuration files.

Configuration Schemes

The configuration data for an APEX 20K device can be loaded with one of five configuration schemes (see Table 65), chosen on the basis of the target application. An EPC2 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of an APEX 20K device. When an EPC2 configuration device is used, the system can configure automatically at system power-up.

Multiple APEX 20K devices can be configured in any of five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

Table 65. Data Sources for Configuration

Configuration Scheme	Data Source
Configuration device	EPC2 configuration device
Passive serial (PS)	MasterBlaster or ByteBlasterMV download cable or serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Passive parallel synchronous (PPS)	Parallel data source
JTAG	MasterBlaster or ByteBlasterMV download cable or a microprocessor with a Jam or JBC File

For more information on configuration, see *Application Note 116 (Configuring APEX 20K, FLEX 10K, & FLEX 6000 Devices.)*

Device Pin-Outs

See the Altera web site **(http://www.altera.com)** or the ***Altera Digital Library*** for pin-out information.

Revision History

The information contained in the *APEX 20K Programmable Logic Device Family Data Sheet version 3.3* supersedes information published in previous versions.

Version 3.3 Change

- Updated Table 5.

Version 3.2 Changes

- Updated Tables 45, 46, 48, 49, 50, 52, 54, 55, 56, 58, 60, and 62

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Problem

What is the ordering code for APEX 20KE devices in a 1,020-pin FineLine BGA™

Solution

The 1,020-pin FineLine BGA package, which supports EP20K600E, EP20K1000E, and EP20K1500E devices, has a new ordering code nomenclature.

Due to the large number of pins on the package, the body size of th be used as the identifying feature, rather than the pin count in th code. For example, the 33-mm wide, 1,020-pin EP20K1500E device in -1 speed grade has an ordering code of EP20K1500EFC33-1.

☞ This new ordering code nomenclature does not affect any other device package.

Feedback

If you have a question or comment about this solution, please enter your name, e-m any comments in the boxes below and then press the **Send my comments** button.

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APEX 20K Device Family Overview

APEX logo

With devices ranging from 30,000 to 1.5 million gates (112,000 to 2.5 million system gates) and clock rates up to 840 MHz, the APEX 20K programmable logic device (PLD) family offers complete system-level integration on a single device, leading to extensive cost and performance advantages. The innovative APEX MultiCore architecture combines and enhances the strengths of previous PLD architectures, delivering the ultimate in design integration and efficiency for high-level, system-on-a-programmable-chip (SOPC) applications.

The APEX 20K device family consists of APEX 20K, APEX 20KE, and APEX 20I devices. To learn more about the differences between them, visit the APEX 20K Features and APEX 20K Architecture pages.

The following tables list the device features of APEX 20KC (1.8 V), APEX 20KE (1.8 V), and APEX 20K (2.5 V) devices.

Table 1. APEX 20KC Device Overview (1.8V)

Device	EP20K100C	EP20K200C	EP20K400C	EP20K600C	EP20K1000C	EP20K150
Typical Gates	100,000	200,000	400,000	600,000	1 million	1.5 millio
Maximum System Gates	269,912	525,824	1,051,648	1,537,024	1,771,520	2,391,184
Logic Elements	4,160	8,320	16,640	24,320	38,400	51,840
Maximum RAM Bits	53,248	106,496	212,992	311,296	327,680	442,368
Phase-Locked Loops (PLLs)	2	2	4	4	4	4
Speed Grades *(1)*	-7, -8, -9	-7, -8, -9	-7, -8, -9	-7, -8, -9	-7, -8, -9	-7, -8, -9

Table 2. APEX 20KE Device Overview (1.8 V) (part 1 of 2)

Device	EP20K30E	EP20K60E	EP20K100E	EP20K160E	EP20K20
Typical Gates	30,000	60,000	100,000	160,000	200,000
Maximum System Gates	122,704	161,792	262,912	404,480	525,824
Logic Elements	1,200	2,560	4,160	6,400	8,320
Maximum RAM Bits	24,576	32,768	53,248	81,920	106,496

Phase-Locked Loops (PLLs)	2	2	2	2	2
Speed Grades *(1)*	-3, -2, -1	-3, -2, -1	-3, -2, -1	-3, -2, -1	-3, -2, -1
Maximum User I/O Pins	128	196	246	316	376
Package (mm)	**Maximum User I/O Pins**				
144-Pin TQFP 20 x 20 *(2)*	92	92	92	88	
144-Pin FineLine BGA Package 20 x 20	93	93	93		
208-Pin PQFP 28 x 28 *(2)*	125	148	151	143	136
208-Pin RQFP 28 x 28 *(2)*					
240-Pin PQFP 32 x 32		151	151	175	168
240-Pin RQFP 32 x 32					
324-Pin FineLine BGA Package 19 x 19	128	196	246		
356-Pin BGA 35 x 35 *(2)*			246	271	271
484-Pin FineLine BGA Package 23 x 23				316	376
652-Pin BGA 45 x 45					376
672-Pin FineLine BGA Package 27 x 27					376
1,020-Pin FineLine BGA Package"F33" 33 x 33					

Table 3. APEX 20KE Device Overview (1.8 V) (part 2 of 2)

Device	EP20K300E	EP20K400E	EP20K600E	EP20K1000E	EP20K150
Typical Gates	300,000	400,000	600,000	1 million	1.5 millio
Maximum System Gates	728,064	1,051,648	1,537,024	1,771,520	2,391,184
Logic Elements	11,520	16,640	24,320	38,400	51,840
Maximum RAM Bits	147,456	212,992	311,296	327,680	442,368
Phase-Locked Loops (PLLs)	4	4	4	4	4
Speed Grades *(1)*	-3, -2, -1	-3, -2, -1	-3, -2, -1	-3, -2, -1	-3, -2, -1
Maximum User I/O Pins	408	488	588	708	808
Package	**Maximum User I/O Pins**				
144-Pin TQFP					

20 x 20 *(2)*					
144-Pin FineLine BGA Package 20 x 20					
208-Pin PQFP 28 x 28 *(2)*					
208-Pin RQFP 28 x 28 *(2)*					
240-Pin PQFP 32 x 32	152				
240-Pin RQFP 32 x 32					
324-Pin FineLine BGA Package 19 x 19					
356-Pin BGA 35 x 35 *(2)*					
484-Pin FineLine BGA Package 23 x 23					
652-Pin BGA 45 x 45	408	488	488	488	488
672-Pin FineLine BGA Package 27 x 27	408	488	508	508	
1,020-Pin FineLine BGA Package"F33" 33 x 33			588	708	808

Table 4. APEX 20K Device Overview (2.5 Volt)			
Device	**EP20K100**	**EP20K200**	**EP20K400**
Maximum System Gates	263,000	526,000	1,052,000
Logic Elements	4,160	8,320	16,640
Maximum RAM bits	53,248	106,496	212,992
Phase-Locked Loops (PLLs)	1	1	1
Speed Grade *(1)*	-3, -2, -1	-3, -2, -1	-3, -2, -1
Maximum User I/O Pins	252	382	502
Package (mm)	**Maximum User I/O Pins**		
144-Pin TQFP 20 x 20	101		
144-Pin FineLine BGA	106		
208-Pin PQFP 28 x 28	159	144	
240-Pin PQFP 28 x 28	189	174	
324-Pin FineLine BGA Package 19 x 19	252		

356-Pin BGA 35 x 35	252	277	
484-Pin FineLine BGA Package 23 x 23		382	
652-Pin BGA 45 x 45			502
672-Pin FineLine BGA Package 27 x 27			502

Notes to Tables:

1. For APEX 20KC devices, -7 is the fastest speed grade; for APEX 20K and APEX 20KE devices -1 is the fastest speed grade.
2. TQFP: thin quad flat pack, PQFP: plastic quad flat pack, RQFP: power quad flat pack, BGA ball-grid array

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Step 3 - Select a Device & Package Option

The next step in selecting the Altera device that best fits your design is to choose the device and the packaging that you require, build the ordering code, and check on the availability of that option.

- Product ordering codes
- Available devices & obsolete ordering codes
- Ordering Altera products
- Development Tools Selector Guide

Product Ordering Codes

Altera devices are offered in a wide variety of pin and package options. For details on available pin counts and speed grades, see the individual device family data sheets. For detailed information on Altera packaging solutions, see the Altera Packages pages.

Altera ordering codes have the following format:

Family Signature	Device Type	Package Type	Operating Temperatures	Pin Count	Speed Grade	Suffix
EP	**20K400**	**F**	**C**	**672**	**-1**	**X**

In the example above, the ordering code is **EP20K400FC672-1X**. The device is an APEX™ (**EP**) **20K400** device in a FineLine BGA™ package (**F**) that operates at commercial temperatures (**C**), has **672** pins and a **-1** speed grade, and features ClockLock,™ClockBoost,and LVDS™ (**X**).

Table 1 gives the key to the ordering codes.

Table 1. Key to Product Ordering Codes

Code Type	Code	Definition
Family Signature	EP	APEX™ 20K, ACEX™1K, Classic™
	EPF	FLEX® 10K, FLEX 6000, FLEX 8000
	EPC	Configuration Devices
	EPM	MAX® 9000, MAX 7000, MAX 3000

Device Type	EP	20K60E, 20K100, 20K100E, 20K160E, 20K200, 20K200E, 20K300E, 20K400, 20K400E, 20K600E, 20K1000E, 20K1500E, 1K10, 1K30, 1K50, 1K100, 600, 610, 900, 910, 1800, 1810
	EPF	10K10A, 10K10, 10K20, 10K30E, 10K30A, 10K30, 10K40, 10K50S, 10K50E, 10K50V, 10K50, 10K70, 10K100E, 10K100A, 10K100B, 10K100, 10K130E, 10K130V, 10K200E, 10K200S, 10K250A 6010A, 6016A, 6016, 6024A 8282A, 8282AV, 8452A, 8636A, 8820A, 81188A, 81500A
	EPC	1064, 1064V, 1213, 1441, 1, 2
	EPM	9320A, 9400, 9480, 9560A 7032AE, 7032B, 7032S, 7064AE, 7064B, 7064S, 7128AE, 7128B, 7128S, 7160S, 7192S, 7256AE, 7256B, 7256S, 7512AE, 7512B 3032A, 3064A, 3128A, 3256A
Package Type	P	Plastic dual in-line package (PDIP)
	L	Plastic J-lead chip carrier (PLCC)
	G	Ceramic pin-grid array (PGA)
	B	Ball-grid array (BGA)
	Q	Plastic quad flat pack (PQFP)
	T	Thin plastic quad flat pack (TQFP)
	R	Power quad flat pack (RQFP)
	F	FineLine™ BGA
	U	Ultra FineLine™ BGA
Operating Temperature	C	Commercial temperature (0 to 70 C)
	I	Industrial temperature (-40 C to 85 C)
Pin Count	Number of pins for devices with different pin-count options	
Speed Grade	See the family data sheets in the current data book for speed/product relationships (e.g., -1, -2, -10, -15).	
Suffix	DX	FLEX 10K100 devices with ClockLock and ClockBoost features
	X	PLL or PLL and LVDS Features in APEX 20K, APEX 20KE,and Flex10KE devices.

	P	PCI compliance
	F	Fixed programming algorithm
	C	Carrier

Available Devices & Obsolete Ordering Codes

To see if the device you need is available, you can search the available devices and package optionsand obsolete ordering codes.

Ordering Altera Products

To find out pricing information and to purchase Altera devices, contact your local distributor. A list of North American and international distributors is available on the Contact page.

Development Tools Selector Guide

You have now reached the end of the Device Selector Guide. The Device Selector Guide was designed to help you select the appropriate Altera device for your design. Starting on the next page you will find the Development Tools Selector Guide, which will help you choose the Altera software environment that best suits your development needs.

Previous page | Next Page

Last updated: Jan. 28, 2001

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Device	Package	Pins	Speed Grade	Temp	Ordering Code *Note (1)*	
EP20K100	BGA	356	-3	C	EP20K100BC356-3	
			-2	C	EP20K100BC356-2	
					EP20K100BC356-2X	
			-1	C	EP20K100BC356-1	
					EP20K100BC356-1X	
				C	EP20K100BC356-1V	
	FineLine BGA	324	-3	C	EP20K100FC324-3	
			-2	C	EP20K100FC324-2	
					EP20K100FC324-2X	
			-1	C	EP20K100FC324-1	
					EP20K100FC324-1X	
				C	EP20K100FC324-3V	
	PQFP	208	-3	C	EP20K100QC208-3	
					EP20K100QC208-3V	
			-2	C	EP20K100QC208-2	
					EP20K100QC208-2X	
				I	EP20K100QI208-2	
			-1	C	EP20K100QC208-1X	
			-1	C	EP20K100QC208-1	
				I	EP20K100QI208-2V	
		240	-3	C	EP20K100QC240-3	
			-2	C	EP20K100QC240-2	

					EP20K100QC240-2X
				I	EP20K100QI240-2
			-1	C	EP20K100QC240-1
					EP20K100QC240-1X
				C	EP20K100QC240-3V
				I	EP20K100QI240-2V
	TQFP	144	-3	C	EP20K100TC144-3
			-2	C	EP20K100TC144-2
					EP20K100TC144-2X
			-1	C	EP20K100TC144-1
					EP20K100TC144-1X
				C	EP20K100TC144-1V
EP20K1000E	BGA	652	-3	C	EP20K1000EBC652-3
			-2	C	EP20K1000EBC652-2
					EP20K1000EBC652-2X
			-1	C	EP20K1000EBC652-1
					EP20K1000EBC652-1X
				C	EP20K1000EBC652XES
	FineLine BGA	33	-1	C	EP20K1000EFC33-1
					EP20K1000EFC33-1X
		672	-3	C	EP20K1000EFC672-3
			-2	C	EP20K1000EFC672-2
					EP20K1000EFC672-2X
			-1	C	EP20K1000EFC672-1
					EP20K1000EFC672-1X
EP20K100E	BGA	356	-3	C	EP20K100EBC356-3

			-2	C	EP20K100EBC356-2
					EP20K100EBC356-2X
			-1	C	EP20K100EBC356-1
					EP20K100EBC356-1X
				C	EP20K100EBC356XES
	FineLine BGA	144	-3	C	EP20K100EFC144-3
			-2	C	EP20K100EFC144-2
					EP20K100EFC144-2X
				I	EP20K100EFI144-2x
			-1	C	EP20K100EFC144-1
					EP20K100EFC144-1X
				C	EP20K100EFC144ES
		324	-3	C	EP20K100EFC324-3
			-2	C	EP20K100EFC324-2
					EP20K100EFC324-2X
				I	EP20K100EFI324-2X
			-1	C	EP20K100EFC324-1
					EP20K100EFC324-1X
				C	EP20K100EFC324XES
	PQFP	208	-2	C	EP20K100EQC208-2X
			-1	C	EP20K100EQC208-1X
				C	EP20K100EQC208XES
		240	-2	C	EP20K100EQC240-2X
	TQFP	144	-2	C	EP20K100ETC144-2X
			-1	C	EP20K100ETC144-1X
				C	EP20K100ETC144XES
EP20K1500E	BGA	652	-3	C	EP20K1500EBC652-3

			-2	C	EP20K1500EBC652-2
			-2X	C	EP20K1500EBC652-2X
			-1	C	EP20K1500EBC652-1
					EP20K1500EBC652-1X
	FineLine BGA	33	-3	C	EP20K1500EFC33-3
			-2	C	EP20K1500EFC33-2
					EP20K1500EFC33-2X
			-1	C	EP20K1500EFC33-1
					EP20K1500EFC33-1X
EP20K160E	BGA	356	-3	C	EP20K160EBC356-3
			-2	C	EP20K160EBC356-2
					EP20K160EBC356-2X
			-1	C	EP20K160EBC356-1
					EP20K160EBC356-1X
	FineLine BGA	484	-3	C	EP20K160EFC484-3
			-2	C	EP20K160EFC484-2
					EP20K160EFC484-2X
			-1	C	EP20K160EFC484-1
					EP20K160EFC484-1X
	PQFP	208	-3	C	EP20K160EQC208-3
			-2	C	EP20K160EQC208-2
					EP20K160EQC208-2X
			-1	C	EP20K160EQC208-1
				C	EP20K160EQC208-3V
					EP20K160EQC208-1X-1
		240	-3	C	EP20K160EQC240-3

			-2	C	EP20K160EQC240-2
					EP20K160EQC240-2X
			-1	C	EP20K160EQC240-1
					EP20K160EQC240-1X
	TQFP	144	-3	C	EP20K160ETC144-3
			-2	C	EP20K160ETC144-2
					EP20K160ETC144-2X
			-1	C	EP20K160ETC144-1
					EP20K160ETC144-1X
EP20K20	RQFP	240		C	EP20K20RC240-3V
EP20K200	BGA	356	-3	C	EP20K200BC356-3
			-2	C	EP20K200BC356-2
					EP20K200BC356-2X
			-1	C	EP20K200BC356-1
					EP20K200BC356-1X
				C	EP20K200BC356-3V
					EP20K200BC356-1XV
	FineLine BGA	484	-2	C	EP20K200FC484-2X
			-1	C	EP20K200FC484-1X
				C	EP20K200FC484-3V
					EP20K200FC484-2XV
				I	EP20K200FI484-2V
	RQFP	208	-3	C	EP20K200RC208-3
			-2	C	EP20K200RC208-2
					EP20K200RC208-2X
			-1	C	EP20K200RC208-1

					EP20K200RC208-1X
				C	EP20K200RC208-1V
		240	-3	C	EP20K200RC240-3
			-2	C	EP20K200RC240-2
					EP20K200RC240-2X
				I	EP20K200RI240-2
			-1	C	EP20K200RC240-1
					EP20K200RC240-1X
				I	EP20K200RI240
					EP20K200RI240-2V
EP20K200E	BGA	356	-3	C	EP20K200EBC356-3
			-2	C	EP20K200EBC356-2
					EP20K200EBC356-2X
			-1	C	EP20K200EBC356-1
					EP20K200EBC356-1X
				C	EP20K200EBC356ES
		652	-3	C	EP20K200EBC652-3
			-2	C	EP20K200EBC652-2
					EP20K200EBC652-2X
			-1	C	EP20K200EBC652-1
					EP20K200EBC652-1X
				C	EP20K200EBC652XES
	FineLine BGA	484	-3	C	EP20K200EFC484-3
			-2	C	EP20K200EFC484-2
					EP20K200EFC484-2X
				C	EP20K200EFC484XES
				I	EP20K200EFI484-2X

		672	-3	C	EP20K200EFC672-3
			-2	C	EP20K200EFC672-2
					EP20K200EFC672-2X
			-1	C	EP20K200EFC672-1
					EP20K200EFC672-1X
				C	EP20K200EFC672XES
	PQFP	208	-3	C	EP20K200EQC208-3
			-2	C	EP20K200EQC208-2
			-1	C	EP20K200EQC208-1
		240	-3	C	EP20K200EQC240-3
			-2	C	EP20K200EQC240-2
				I	EP20K200EQI240-2
			-1	C	EP20K200EQC240-1
				C	EP20K200EQC240ES
EP20K300E	BGA	652	-3	C	EP20K300EBC652-3
			-2	C	EP20K300EBC652
			-2	C	EP20K300EBC652-2X
			-1	C	EP20K300EBC652-1
					EP20K300EBC652-1X
				C	EP20K300EBC652XES
	FineLine BGA	672	-3	C	EP20K300EFC672-3
			-2	C	EP20K300EFC672-2
					EP20K300EFC672-2X
				I	EP20K300EFI672-2x
			-1	C	EP20K300EFC672-1
					EP20K300EFC672-1X

				C	EP20K300EFC672XES
	PQFP	240	-3	C	EP20K300EQC240-3
			-2	C	EP20K300EQC240-2
					EP20K300EQC240-2X
			-1	C	EP20K300EQC240-1
					EP20K300EQC240-1X
				C	EP20K300EQC240XES
EP20K30E	FineLine BGA	144	-3	C	EP20K30EFC144-3
			-2	C	EP20K30EFC144-2
					EP20K30EFC144-2X
				I	EP20K30EFI144-2X
			-1	C	EP20K30EFC144-1
					EP20K30EFC144-1X
		324	-3	C	EP20K30EFC324-3
			-2	C	EP20K30EFC324-2
					EP20K30EFC324-2X
			-1	C	EP20K30EFC324-1X
	PQFP	208	-3	C	EP20K30EQC208-3
			-2	C	EP20K30EQC208-2
					EP20K30EQC208-2X
			-1	C	EP20K30EQC208-1
					EP20K30EQC208-1X
	TQFP	144	-3	C	EP20K30ETC144-3
			-2	C	EP20K30ETC144-2
					EP20K30ETC144-2X
			-1	C	EP20K30ETC144-1
					EP20K30ETC144-1X

EP20K400	BGA	652	-3	C	EP20K400BC652-3
			-2	C	EP20K400BC652-2X
				I	EP20K400BI652-2
			-1	C	EP20K400BC652-1
					EP20K400BC652-1X
				C	EP20K400BC652-3V
					EP20K400BC652-2XV
	FineLine BGA	672	-3	C	EP20K400FC672-3
			-2	C	EP20K400FC672-2
					EP20K400FC672-2X
				I	EP20K400FI672-2
					EP20K400FI672-2V
			-1	C	EP20K400FC672-1
					EP20K400FC672-1X
				C	EP20K400FC672-3V
					EP20K400FC672-2XV
	PGA	655	-3	C	EP20K400GC655-3
			-2	C	EP20K400GC655-2
			-1	C	EP20K400GC655-1
EP20K400E	BGA	652	-3	C	EP20K400EBC652-3
			-2	C	EP20K400EBC652-2
					EP20K400EBC652-2X
				I	EP20K400EBI652-2X
			-1	C	EP20K400EBC652-1
					EP20K400EBC652-1X
	FineLine BGA	672	-2	C	EP20K400EFC672-2

					EP20K400EFC672-2X
				I	EP20K400EFI672-2X
			-1	C	EP20K400EFC672-1
					EP20K400EFC672-1X
EP20K600E	BGA	652	-3	C	EP20K600EBC652-3
			-2	C	EP20K600EBC652-2
					EP20K600EBC652-2X
			-1	C	EP20K600EBC652-1
					EP20K600EBC652-1X
				C	EP20K600EBC652XES
	FineLine BGA	33	-3	C	EP20K600EFC33-3
			-2	C	EP20K600EFC33-2
					EP20K600EFC33-2X
			-1	C	EP20K600EFC33-1
					EP20K600EFC33-1X
				C	EP20K600EFC33-2X-2
		672	-3	C	EP20K600EFC672-3
			-2	C	EP20K600EFC672-2
					EP20K600EFC672-2X
			-1	C	EP20K600EFC672-1
					EP20K600EFC672-1X
				C	EP20K600EFC672XES
EP20K60E	BGA	324	-1	C	EP20K60EBC324-1X
		356	-3	C	EP20K60EBC356-3
			-2	C	EP20K60EBC356-2
					EP20K60EBC356-2X
			-1	C	EP20K60EBC356-1

					EP20K60EBC356-1X
	FineLine BGA	144	-3	C	EP20K60EFC144-3
			-2	C	EP20K60EFC144-2
					EP20K60EFC144-2X
			-1	C	EP20K60EFC144-1
					EP20K60EFC144-1X
		324	-3	C	EP20K60EFC324-3
			-2	C	EP20K60EFC324-2
			-1	C	EP20K60EFC324-1
				C	EP20K60EFC324-2X
	PQFP	208	-3	C	EP20K60EQC208-3
			-2	C	EP20K60EQC208-2
					EP20K60EQC208-2X
			-1	C	EP20K60EQC208-1
					EP20K60EQC208-1X
		240	-3	C	EP20K60EQC240-3
			-2	C	EP20K60EQC240-2
					EP20K60EQC240-2X
			-1	C	EP20K60EQC240-1
				C	EP20K60EQC240-1X
	TQFP	144	-3	C	EP20K60ETC144-3
			-2	C	EP20K60ETC144-2
			-1	C	EP20K60ETC144-1
				C	EP20K60ETC144-2X
					EP20K60ETC144-1X-1

Note:
1. For an explanation of Altera ordering codes, refer to Product Ordering Codes .

2. C: device is shipped in a carrier. DX or X: device has the ClockLock and ClockI features. F: device supports fixed programming algorithms for in-circuit testers. P: is PCI-compliant.

Enter a new search below:

Choose a device family:

- ☐ ACEX 1K
- ☐ APEX 20K
- ☐ FLEX 10K
- ☐ FLEX 8000
- ☐ FLEX 6000
- ☐ MAX 9000
- ☐ MAX 7000
- ☐ MAX 3000A
- ☐ Classic
- ☐ Configuration EPROM

Choose a package:

- ☑ Any available package
- ☐ Ceramic dual in-line package (CerDIP)
- ☐ Plastic dual in-line package (PDIP)
- ☐ Plastic small-outline integrated circuit (SOIC)
- ☐ Ceramic J-lead chip carrier (JLCC)
- ☐ Plastic J-lead chip carrier (PLCC)
- ☐ Thin plastic quad flat pack (TQFP)
- ☐ Plastic quad flat pack (PQFP)
- ☐ Power quad flat pack (RQFP)
- ☐ Ceramic quad flat pack (CQFP)
- ☐ Ceramic pin-grid array (PGA)
- ☐ Ball-grid array (BGA)
- ☐ FineLine BGA

You can type options in the box below (e.g., speed grade)

Send It Clear Form

Last updated: November 28, 2000

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New APEX 20KE
Device Ordering Codes

April 2000, ver. 1 Errata Sheet

Preliminary Information

This errata sheet provides new ordering code information for APEX™ 20KE devices. Altera is developing a faster process for APEX 20KE devices that will meet the timing specification for production -1 and -1X speed-grade devices.

In the interim, Altera is offering engineering sample (ES) devices for -1 and -1X speed-grade APEX 20KE devices. These ES devices have slower timing characteristics when operating under worst-case conditions (85 °C and 1.71 V) than what is reflected in the Quartus software for the -1 and -1X speed-grade devices. However, these devices should meet the timing specifications shown in the Quartus software under typical lab operating conditions.

APEX 20KE ES devices in -1 and -1X speed grades do not have the "-1" speed-grade identifier in the ordering code. Instead, an "ES" or "XES" is appended to the end of the ordering code. For example, the EP20K100ETC144-1 and EP20K100ETC144-1X device ES ordering codes are EP20K100ETC144ES and EP20K100ETC144XES, respectively.

Additionally, APEX 20KE ES devices in -1 and -1X speed grades are marked in one of two ways. Most of these ES devices are marked with the complete ordering code (i.e., including the "-1") with an "ES" appended to the end. For example, the EP20K100ETC144-1 and EP20K100ETC144-1X ES devices have EP20K100ETC144-1ES and EP20K100ETC144-1XES markings, respectively. However, a small number of devices are marked with the exact ordering code (i.e., without the "-1"). Table 1 lists the new ordering codes and markings for -1 and -1X speed-grade APEX 20KE ES devices.

Table 1. Ordering Codes for APEX 20KE ES Devices in -1 & -1X Speed Grades

Device	Package *(1)*	Ordering Code Example	Device Marking Example 1	Device Marking Example 2
EP20K100E	144-pin TQFP, 144-pin FineLine BGA™, 208-pin PQFP, 240-pin PQFP, 324-pin FineLine BGA, 356-pin BGA	EP20K100ETC144ES	EP20K100ETC144-1ES	EP20K100ETC144ES
		EP20K100ETC144XES	EP20K100ETC144-1XES	EP20K100ETC144XES
EP20K200E	208-pin PQFP, 240-pin PQFP, 356-pin BGA, 484-pin FineLine BGA, 652-pin BGA, 672-pin FineLine BGA	EP20K200EFC672ES	EP20K200EFC672-1ES	EP20K200EFC672ES
		EP20K200EFC672XES	EP20K200EFC672-1XES	EP20K200EFC672XES
EP20K300E	240-pin PQFP, 652-pin BGA, 672-pin FineLine BGA	EP20K300EFC672ES	EP20K300EFC672-1ES	EP20K300EFC672ES
		EP20K300EFC672XES	EP20K300EFC672-1XES	EP20K300EFC672XES
EP20K600E	652-pin BGA, 672-pin FineLine BGA, 1,020-pin FineLine BGA	EP20K600EFC672ES	EP20K600EFC672-1ES	EP20K600EFC672ES
		EP20K600EFC672XES	EP20K600EFC672-1XES	EP20K600EFC672XES
EP20K1000E	652-pin BGA, 672-pin FineLine BGA, 1,020-pin FineLine BGA	EP20K1000EFC672ES	EP20K1000EFC672-1ES	EP20K1000EFC672ES
		EP20K1000EFC672XES	EP20K1000EFC672-1XES	EP20K1000EFC672XES

Note:
(1) TQFP: thin quad flat pack; PQFP: plastic quad flat pack; BGA: ball-grid array.

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Altera Device Package Information

August 2000, ver. 8.03 Data Sheet

Introduction

This data sheet provides the following package information for all Altera® devices:

- Lead materials
- Thermal resistance
- Package weights
- Package outlines

In this data sheet, packages are listed in order of ascending pin count.

Lead Materials

Table 1 shows the available package types, package acronyms, lead materials, and lead finishes for all Altera device packages.

Table 1. Altera Device Lead Materials

Package Type	Package Acronym	Lead Material	Lead Finish *(1)*
Ceramic dual in-line	CerDIP	Alloy 42	Solder dip
Plastic dual in-line	PDIP	Copper	Solder plate
Ceramic J-lead chip carrier	JLCC	Alloy 42	Solder dip
Plastic J-lead chip carrier	PLCC	Copper	Solder plate
Ceramic pin-grid array *(2)*	PGA	Alloy 42	Gold over nickel plate
Plastic small-outline integrated circuit	SOIC	Copper	Solder plate
Plastic quad flat pack	PQFP	Copper	Solder plate
Plastic thin quad flat pack	TQFP	Copper	Solder plate
Power quad flat pack	RQFP	Copper	Solder plate
Ball-grid array	BGA	Tin-lead alloy (63/37)	–
FineLine BGA™	FineLine BGA	Tin-lead alloy (63/37)	–
Ultra FineLine BGA™	Ultra FineLine BGA	Tin-lead alloy (63/37)	–

Notes:
(1) Solder dip lead finishes are 60/40 typical, and solder plate lead finished are 85/15 typical.
(2) An industry-standard lead glass called T-187 (lead oxide glass) is used to seal PGA packages. This material is manufactured by Sumitomo Corporation.

Thermal Resistance

Tables 2 through 11 provide θ_{JA} (junction-to-ambient thermal resistance) and θ_{JC} (junction-to-case thermal resistance) values for Altera APEX™ 20K and APEX 20KE, FLEX® 10K and FLEX 10KE, FLEX 8000, FLEX 6000, MAX® 9000, MAX 7000, MAX 5000, MAX 3000A, Classic™, and configuration devices.

Table 2. Thermal Resistance of APEX 20K & APEX 20KE Devices (Part 1 of 2)

Device	Pin Count	Package	θ_{JC} (° C/W)	θ_{JA} (° C/W) Still Air	θ_{JA} (° C/W) 100 ft./min.	θ_{JA} (° C/W) 200 ft./min.	θ_{JA} (° C/W) 400 ft./min.
EP20K60E	144	TQFP	9.0	33.0	26.0	22.0	20.0
	196	FineLine BGA	6.3	30.6	29.5	28.2	25.4
	208	PQFP	7.0	35.0	24.0	18.0	14.0
	240	PQFP	7.0	30.0	22.0	17.0	14.0
	324	Fineline BGA	5.8	27.6	26.3	24.9	22.2
	356	BGA	2.0	15.0	12.0	9.0	8.0
EP20K100 EP20K100E	144	TQFP	9.0	33.0	26.0	22.0	20.0
	196	FineLine BGA	6.3	30.6	29.5	28.2	25.4
	208	PQFP	7.0	35.0	24.0	18.0	14.0
	240	PQFP	7.0	30.0	22.0	17.0	14.0
	324	FineLine BGA	5.8	27.6	26.3	24.9	22.2
	356	BGA	2.0	15.0	12.0	9.0	8.0
EP20K160E	144	TQFP	9.0	33.0	26.0	22.0	20.0
	208	PQFP	7.0	35.0	24.0	18.0	14.0
	240	PQFP	7.0	30.0	22.0	17.0	14.0
	356	BGA	2.0	15.0	12.0	9.0	8.0
	484	FineLine BGA	6.0	21.0	17.0	14.0	13.0
EP20K200	208	RQFP	2.0	18.0	12.0	9.0	7.0
	240	RQFP	2.0	20.0	13.0	10.0	8.0
	356	BGA	2.0	15.0	12.0	9.0	8.0
	484	FineLine BGA	6.0	21.0	17.0	14.0	13.0
EP20K200E	208	PQFP	7.0	35.0	24.0	18.0	14.0
	240	PQFP	7.0	30.0	22.0	17.0	14.0
	356	BGA	2.0	15.0	12.0	9.0	8.0
	484	FineLine BGA	6.0	21.0	17.0	14.0	13.0
	652	BGA	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*
	672	FineLine BGA	5.2	17.5	17.1	16.8	16.3
EP20K300E	208	RQFP	2.0	18.0	12.0	9.0	7.0
	240	RQFP	2.0	20.0	13.0	10.0	8.0
	652	BGA	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*
	672	FineLine BGA	5.2	17.5	17.1	16.8	16.3

Table 2. Thermal Resistance of APEX 20K & APEX 20KE Devices (Part 2 of 2)

Device	Pin Count	Package	θ_{JC} (° C/W)	θ_{JA} (° C/W) Still Air	θ_{JA} (° C/W) 100 ft./min.	θ_{JA} (° C/W) 200 ft./min.	θ_{JA} (° C/W) 400 ft./min.
EP20K400	652	BGA	2.0	13.0	10.0	8.0	7.0
	655	PGA	1.0	8.0	7.0	6.0	4.0
	672	FineLine BGA	5.2	17.5	17.1	16.8	16.3
	672	Flip Chip	0.3	12.3	6.7	5.7	4.8
	672	Flip Chip w/ fin	0.3	6.7	4.1	3.3	2.6
EP20K400E	652	BGA	2.0	13.0	10.0	8.0	7.0
	672	FineLine BGA	4.8	19.0	18.0	17.0	16.0
	672	Flip Chip	0.3	12.3	6.7	5.7	4.8
	672	Flip Chip w/ fin	0.3	6.7	4.1	3.3	2.6
EP20K600E	652	BGA	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*
	672	FineLine BGA	4.8	18.0	17.0	16.0	15.0
	672	Flip Chip	0.3	11.7	6.6	5.8	4.7
	672	Flip Chip w/ fin	0.3	6.2	4.0	3.2	2.5
	1,020	FineLine BGA	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*
	1,020	Flip Chip	0.3	10.7	6.1	5.1	4.2
	1,020	Flip Chip w/ fin	0.3	5.1	3.4	2.7	2.2
EP20K1000E	652	BGA	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*
	652	Flip Chip	0.2	9.1	5.9	4.8	4.0
	652	Flip Chip w/ fin	0.2	3.4	2.7	2.1	1.7
	672	FineLine BGA	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*
	672	Flip Chip	0.2	10.9	6.4	5.4	4.5
	672	Flip Chip w/ fin	0.2	5.7	3.9	3.1	2.4
	984	PGA	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*
	1,020	FineLine BGA	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*
EP20K1500E	652	BGA	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*
	652	Flip Chip	0.2	8.7	5.8	4.7	3.9
		Flip Chip w/ fin	0.2	3.4	3.2	2.5	2.0
	984	PGA	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*
	1,020	FineLine BGA	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*
	1.020	Flip Chip	0.2	9.4	5.8	4.8	3.9
	1,020	Flip Chip w/ fin	0.2	4.4	3.3	2.5	2.0

Note:
(1) For thermal resistance values, contact Altera Applications.

Table 3. Thermal Resistance of FLEX 10K Devices (Part 1 of 3) *Note (1)*

Device	Pin Count	Package	θ_{JC} (° C/W)	θ_{JA} (° C/W) Still Air	θ_{JA} (° C/W) 100 ft./min.	θ_{JA} (° C/W) 200 ft./min.	θ_{JA} (° C/W) 400 ft./min.
EPF10K10	84	PLCC	11.0	35.0	23.0	18.0	14.0
	144	TQFP	9.0	33.0	26.0	22.0	20.0
	208	PQFP	7.0	35.0	24.0	18.0	14.0
EPF10K10A	100	TQFP	10.0	44.0	38.0	34.0	31.0
	144	TQFP	9.0	33.0	26.0	22.0	20.0
	208	PQFP	7.0	35.0	24.0	18.0	14.0
	256	FineLine BGA	**6.7**	**33.0**	**30.0**	**28.0**	**26.0**
EPF10K20	144	TQFP	9.0	33.0	26.0	22.0	20.0
	208	RQFP	2.0	18.0	12.0	9.0	7.0
	240	RQFP	2.0	20.0	13.0	10.0	8.0
EPF10K30	208	RQFP	2.0	18.0	12.0	9.0	7.0
	240	RQFP	2.0	20.0	13.0	10.0	8.0
	356	BGA	2.0	15.0	12.0	9.0	8.0
EPF10K30A	144	TQFP	9.0	33.0	26.0	22.0	20.0
	208	PQFP	7.0	35.0	24.0	18.0	14.0
	240	PQFP	7.0	30.0	22.0	17.0	14.0
	256	FineLine BGA	**5.7**	**28.0**	**26.0**	**24.0**	**23.0**
	356	BGA	2.0	15.0	12.0	9.0	8.0
	484	FineLine BGA	**5.4**	**23.9**	**22.0**	**20.7**	**19.5**
EPF10K30E	144	TQFP	9.0	33.0	26.0	22.0	20.0
	208	PQFP	7.0	35.0	24.0	18.0	14.0
	256	FineLine BGA	**5.7**	**28.0**	**26.0**	**24.0**	**23.0**
	484	FineLine BGA	**5.4**	**23.9**	**22.0**	**20.7**	**19.5**
EPF10K40	208	RQFP	2.0	18.0	12.0	9.0	7.0
	240	RQFP	2.0	20.0	13.0	10.0	8.0
EPF10K50	240	RQFP	2.0	20.0	13.0	10.0	8.0
	356	BGA	2.0	15.0	12.0	9.0	8.0
	403	PGA	**3.0**	**12.0**	**10.0**	**9.0**	**8.0**
		PGA *(2)*	**3.0**	**10.0**	**8.0**	**7.0**	**6.0**
EPF10K50V	240	RQFP	2.0	20.0	13.0	10.0	8.0
	356	BGA	2.0	15.0	12.0	9.0	8.0
	484	FineLine BGA	4.9	23.0	22.0	21.5	20.0

Table 3. Thermal Resistance of FLEX 10K Devices (Part 2 of 3) *Note (1)*

Device	Pin Count	Package	θ_{JC} (° C/W)	θ_{JA} (° C/W) Still Air	θ_{JA} (° C/W) 100 ft./min.	θ_{JA} (° C/W) 200 ft./min.	θ_{JA} (° C/W) 400 ft./min.
EPF10K50E	144	TQFP	9.0	33.0	26.0	22.0	20.0
	208	PQFP	7.0	35.0	24.0	18.0	14.0
	240	PQFP	7.0	30.0	22.0	17.0	14.0
	256	FineLine BGA	7.1	29.7	28.0	26.6	24.0
	356	BGA	2.0	15.0	12.0	9.0	8.0
	484	FineLine BGA	5.5	23.5	22.2	21.0	19.2
EPF10K50S	144	TQFP	9.0	33.0	26.0	22.0	20.0
	208	PQFP	7.0	35.0	24.0	18.0	14.0
	240	PQFP	7.0	30.0	22.0	17.0	14.0
	256	FineLine BGA	7.1	29.7	28.0	26.6	24.0
	356	BGA	2.0	15.0	12.0	9.0	8.0
	484	FineLine BGA	5.4	25.0	24.0	23.0	21.5
EPF10K70	240	RQFP	2.0	20.0	13.0	10.0	8.0
	503	PGA	1.0	8.0	7.0	6.0	4.0
EPF10K100	503	PGA	**1.0**	**8.0**	**7.0**	**6.0**	**4.0**
		PGA *(2)*	1.0	6.0	5.0	4.0	3.0
		PGA *(3)*	–	**2.0**	–	–	–
EPF10K100A	240	RQFP	2.0	20.0	13.0	10.0	8.0
	356	BGA	2.0	15.0	12.0	9.0	8.0
	484	FineLine BGA	5.2	21.7	20.6	19.6	18.2
	600	BGA	2.0	13.0	10.0	8.0	7.0
EPF10K100E	208	PQFP	7.0	35.0	24.0	18.0	14.0
	240	PQFP	7.0	30.0	22.0	17.0	14.0
	256	FineLine BGA	5.6	28.8	27.5	26.1	23.4
	356	BGA	2.0	15.0	12.0	9.0	8.0
	484	FineLine BGA	5.4	23.0	21.8	20.7	18.9
EPF10K130V	599	PGA	1.0	8.0	7.0	6.0	4.0
	600	BGA	2.0	13.0	10.0	8.0	7.0
EPF10K130E	240	PQFP	7.0	30.0	22.0	17.0	14.0
	356	BGA	2.0	15.0	12.0	9.0	8.0
	484	FineLine BGA	5.3	22.4	21.2	20.2	18.5
	600	BGA	2.0	13.0	10.0	8.0	7.0
	672	FineLine BGA	5.2	18.9	18.2	17.6	16.9
EPF10K200E	599	PGA	1.0	8.0	7.0	6.0	4.0
	600	BGA	2.0	13.0	10.0	8.0	7.0
	672	FineLine BGA	5.2	17.8	17.3	17.0	16.4

Table 3. Thermal Resistance of FLEX 10K Devices (Part 3 of 3) *Note (1)*

Device	Pin Count	Package	θ_{JC} (° C/W)	θ_{JA} (° C/W) Still Air	θ_{JA} (° C/W) 100 ft./min.	θ_{JA} (° C/W) 200 ft./min.	θ_{JA} (° C/W) 400 ft./min.
EPF10K200S	240	RQFP	2.0	20.0	13.0	10.0	8.0
	356	BGA	2.0	15.0	12.0	9.0	8.0
	484	FineLine BGA	6.0	21.0	17.0	14.0	13.0
	600	BGA	2.0	13.0	10.0	8.0	7.0
	672	FineLine BGA	4.8	20.0	19.7	19.4	19.0
EPF10K250A	599	PGA	1.0	8.0	7.0	6.0	4.0
	600	BGA	2.0	13.0	10.0	8.0	7.0

Notes:
(1) Bold type designates measured values. FLEX 10KA and FLEX 10KE devices are not measured.
(2) Attached pin-fin heat sink.
(3) Attached motor driven fan heat sink.

Table 4. Thermal Resistance of FLEX 8000 Devices *Note (1)*

Device	Pin Count	Package	θ_{JC} (° C/W)	θ_{JA} (° C/W) Still Air	θ_{JA} (° C/W) 100 ft./min.	θ_{JA} (° C/W) 200 ft./min.	θ_{JA} (° C/W) 400 ft./min.
EPF8282A	84	PLCC	**11.0**	**35.0**	**23.0**	**18.0**	**14.0**
	100	TQFP	**10.0**	**44.0**	**38.0**	**34.0**	**31.0**
EPF8282AV	100	TQFP	**10.0**	**44.0**	**38.0**	**34.0**	**31.0**
EPF8452A	84	PLCC	**11.0**	**35.0**	**23.0**	**18.0**	**14.0**
	100	TQFP	**10.0**	**44.0**	**38.0**	**34.0**	**31.0**
	160	PQFP	**7.0**	**35.0**	**26.0**	**20.0**	**16.0**
	160	PGA	**6.0**	**20.0**	**13.0**	**10.0**	**8.0**
EPF8636A	84	PLCC	**11.0**	**35.0**	**23.0**	**18.0**	**14.0**
	160	PQFP	**6.0**	**20.0**	**13.0**	**10.0**	**8.0**
	192	PGA	**6.0**	**16.0**	**11.0**	**8.0**	**6.0**
	208	PQFP	7.0	35.0	24.0	18.0	14.0
	208	RQFP	**2.0**	**18.0**	**12.0**	**9.0**	**7.0**
EPF8820A	144	TQFP	9.0	33.0	26.0	22.0	20.0
	160	PQFP	**6.0**	**20.0**	**13.0**	**10.0**	**8.0**
	192	PGA	**6.0**	**16.0**	**11.0**	**8.0**	**6.0**
	208	PQFP	7.0	35.0	24.0	18.0	14.0
	208	RQFP	**2.0**	**18.0**	**12.0**	**9.0**	**7.0**
	225	BGA	**6.0**	**28.0**	**19.0**	**14.0**	**11.0**
EPF81188A	208	PQFP	7.0	35.0	24.0	18.0	14.0
	232	PGA	**2.0**	**14.0**	**10.0**	**7.0**	**5.0**
	240	PQFP	**7.0**	**30.0**	**22.0**	**17.0**	**14.0**
	240	RQFP	**2.0**	**20.0**	**13.0**	**10.0**	**8.0**
EPF81500A	240	PQFP	**7.0**	**30.0**	**22.0**	**17.0**	**14.0**
	240	RQFP	**2.0**	**20.0**	**13.0**	**10.0**	**8.0**
	280	PGA	**2.0**	**14.0**	**10.0**	**7.0**	**5.0**
	304	RQFP	**1.0**	**20.0**	**13.0**	**10.0**	**8.0**

Note:
(1) Bold type designates measured values.

Table 5. Thermal Resistance of FLEX 6000 Devices

Device	Pin Count	Package	θ_{JC} (° C/W)	θ_{JA} (° C/W) Still Air	θ_{JA} (° C/W) 100 ft./min.	θ_{JA} (° C/W) 200 ft./min.	θ_{JA} (° C/W) 400 ft./min.
EPF6010A	100	TQFP	10.0	44.0	38.0	34.0	31.0
	144	TQFP	9.0	33.0	26.0	22.0	20.0
EPF6016	144	TQFP	9.0	33.0	26.0	22.0	20.0
	208	PQFP	7.0	35.0	24.0	18.0	14.0
	240	PQFP	7.0	30.0	22.0	17.0	14.0
	256	BGA	6.0	28.0	22.0	20.0	19.0
EPF6016A	100	TQFP	10.0	44.0	38.0	34.0	31.0
		FineLine BGA	10.0	33.0	29.0	26.0	24.0
	144	TQFP	9.0	33.0	26.0	22.0	20.0
	208	PQFP	7.0	35.0	24.0	18.0	14.0
	256	FineLine BGA	9.0	27.0	23.0	21.0	19.0
EPF6024A	144	TQFP	9.0	33.0	26.0	22.0	20.0
	208	PQFP	7.0	35.0	24.0	18.0	14.0
	240	PQFP	7.0	30.0	22.0	17.0	14.0
	256	BGA	6.0	28.0	22.0	20.0	19.0
		FineLine BGA	9.0	27.0	23.0	21.0	19.0

Table 6. Thermal Resistance of MAX 9000 Devices *Notes (1), (2)*

Device	Pin Count	Package	θ_{JC} (° C/W)	θ_{JA} (° C/W) Still Air	θ_{JA} (° C/W) 100 ft./min.	θ_{JA} (° C/W) 200 ft./min.	θ_{JA} (° C/W) 400 ft./min.
EPM9320	84	PLCC	**11.0**	**35.0**	**23.0**	**18.0**	**14.0**
	208	RQFP	**2.0**	**18.0**	**12.0**	**9.0**	**7.0**
	280	PGA	**2.0**	**14.0**	**10.0**	**7.0**	**5.0**
	356	BGA	2.0	15.0	12.0	9.0	8.0
EPM9320A	84	PLCC	**11.0**	**35.0**	**23.0**	**18.0**	**14.0**
	208	RQFP	**2.0**	**18.0**	**12.0**	**9.0**	**7.0**
	356	BGA	2.0	15.0	12.0	9.0	8.0
EPM9400	84	PLCC	**11.0**	**35.0**	**23.0**	**18.0**	**14.0**
	208	RQFP	**2.0**	**18.0**	**12.0**	**9.0**	**7.0**
	240	RQFP	**2.0**	**20.0**	**13.0**	**10.0**	**8.0**
EPM9480	208	RQFP	**2.0**	**18.0**	**12.0**	**9.0**	**7.0**
	240	RQFP	**2.0**	**20.0**	**13.0**	**10.0**	**8.0**
EPM9560	208	RQFP	**2.0**	**18.0**	**12.0**	**9.0**	**7.0**
	240	RQFP	**2.0**	**20.0**	**13.0**	**10.0**	**8.0**
	280	PGA	**2.0**	**14.0**	**10.0**	**7.0**	**5.0**
	304	RQFP	1.0	20.0	13.0	10.0	8.0
	356	BGA	2.0	15.0	12.0	9.0	8.0
EPM9560A	208	RQFP	**2.0**	**18.0**	**12.0**	**9.0**	**7.0**
	240	RQFP	**2.0**	**20.0**	**13.0**	**10.0**	**8.0**
	304	RQFP	1.0	20.0	13.0	10.0	8.0
	356	BGA	2.0	15.0	12.0	9.0	8.0

Notes:
(1) Bold type designates measured values.
(2) Thermal resistance values for MAX 9000 devices are preliminary.

Table 7. Thermal Resistance of MAX 7000 Devices (Part 1 of 4) *Notes (1), (2)*

Device	Pin Count	Package	θ_{JC} (° C/W)	θ_{JA} (° C/W) Still Air	θ_{JA} (° C/W) 100 ft./min.	θ_{JA} (° C/W) 200 ft./min.	θ_{JA} (° C/W) 400 ft./min.
EPM7032	44	PLCC	9.0	52.0	45.0	41.0	36.0
		PQFP	18.0	63.0	55.0	48.0	43.0
		TQFP	19.0	64.0	56.0	50.0	45.0
EPM7032B	44	PLCC	9.0	52.0	45.0	41.0	36.0
		TQFP	19.0	64.0	56.0	50.0	45.0
	49	Ultra FineLine BGA	23.0	69.0	67.0	66.0	62.0

Table 7. Thermal Resistance of MAX 7000 Devices (Part 2 of 4) *Notes (1), (2)*

Device	Pin Count	Package	θ_{JC} (° C/W)	θ_{JA} (° C/W) Still Air	θ_{JA} (° C/W) 100 ft./min.	θ_{JA} (° C/W) 200 ft./min.	θ_{JA} (° C/W) 400 ft./min.
EPM7032S	44	PLCC	9.0	52.0	45.0	41.0	36.0
		TQFP	19.0	64.0	56.0	50.0	45.0
EPM7032AE	44	PLCC	9.0	52.0	45.0	41.0	36.0
		TQFP	19.0	64.0	56.0	50.0	45.0
EPM7064S	44	PLCC	9.0	52.0	45.0	41.0	36.0
		TQFP	19.0	64.0	56.0	50.0	45.0
	84	PLCC	**11.0**	**35.0**	**23.0**	**18.0**	**14.0**
	100	TQFP	10.0	44.0	38.0	34.0	31.0
EPM7064	44	PLCC	9.0	52.0	45.0	41.0	36.0
		TQFP	19.0	64.0	56.0	50.0	45.0
	68	PLCC	**12.0**	**44.0**	33.0	25.0	20.0
	84	PLCC	**11.0**	**35.0**	**23.0**	**18.0**	**14.0**
	100	PQFP	**11.0**	**50.0**	43.0	38.0	34.0
EPM7064AE EPM7064B	44	PLCC	9.0	52.0	45.0	41.0	36.0
		TQFP	19.0	64.0	56.0	50.0	45.0
	49	Ultra FineLine BGA	23.0	65.0	63.0	61.0	57.0
	100	TQFP	10.0	44.0	38.0	34.0	31.0
		FineLine BGA	**25.2**	**65.0**	**61.0**	**58.0**	**55.0**
EPM7096	68	PLCC	**12.0**	44.0	33.0	25.0	20.0
	84	PLCC	11.0	35.0	23.0	18.0	14.0
	100	PQFP	**11.0**	**50.0**	43.0	38.0	34.0
EPM7128A	84	PLCC	**11.0**	**35.0**	**23.0**	**18.0**	**14.0**
	100	TQFP	10.0	44.0	38.0	34.0	31.0
		FineLine BGA	**14.7**	**42.0**	**39.0**	**37.0**	**36.0**
	144	TQFP	9.0	33.0	26.0	22.0	20.0
	256	FineLine BGA	9.4	35.0	33.3	31.6	28.0
EPM7128B	49	Ultra FineLine BGA	22.0	56.0	54.0	52.0	47.0
	100	TQFP	10.0	44.0	38.0	34.0	31.0
		FineLine BGA	10.0	33.0	29.0	26.0	24.0
	144	TQFP	9.0	33.0	26.0	22.0	20.0
	169	Ultra FineLine BGA	17.0	51.0	49.0	46.0	42.0
	256	FineLine BGA	9.0	27.0	23.0	21.0	19.0

Table 7. Thermal Resistance of MAX 7000 Devices (Part 3 of 4) *Notes (1), (2)*

Device	Pin Count	Package	θ_{JC} (° C/W)	θ_{JA} (° C/W) Still Air	θ_{JA} (° C/W) 100 ft./min.	θ_{JA} (° C/W) 200 ft./min.	θ_{JA} (° C/W) 400 ft./min.
EPM7128E	84	PLCC	**11.0**	**35.0**	**23.0**	**18.0**	**14.0**
	100	PQFP	11.0	50.0	43.0	38.0	34.0
	160	PQFP	**7.0**	**35.0**	**26.0**	**20.0**	**16.0**
EPM7128S	84	PLCC	**11.0**	**35.0**	**23.0**	**18.0**	**14.0**
	100	TQFP	10.0	44.0	38.0	34.0	31.0
		PQFP	11.0	50.0	43.0	38.0	34.0
	160	PQFP	**7.0**	**35.0**	**26.0**	**20.0**	**16.0**
EPM7128AE	84	PLCC	**11.0**	**35.0**	**23.0**	**18.0**	**14.0**
	100	TQFP	10.0	44.0	38.0	34.0	31.0
		FineLine BGA	**19.3**	**50.1**	**47.9**	**45.6**	**41.1**
	144	TQFP	9.0	33.0	26.0	22.0	20.0
	169	Ultra FineLine BGA	16.0	47.0	45.0	43.0	38.0
	256	FineLine BGA	**12.9**	**43.6**	**41.4**	**39.2**	**35.3**
EPM7160E	84	PLCC	**11.0**	**35.0**	**23.0**	**18.0**	**14.0**
	100	PQFP	**11.0**	**50.0**	43.0	38.0	34.0
	160	PQFP	**7.0**	**35.0**	**26.0**	**20.0**	**16.0**
EPM7160S	84	PLCC	**11.0**	**35.0**	**23.0**	**18.0**	**14.0**
	100	TQFP	10.0	44.0	38.0	34.0	31.0
	160	PQFP	**7.0**	**35.0**	**26.0**	**20.0**	**16.0**
EPM7192S	160	PQFP	**7.0**	**35.0**	**26.0**	**20.0**	**16.0**
EPM7192E	160	PGA	**6.0**	**20.0**	**13.0**	**10.0**	**8.0**
		PQFP	**7.0**	**35.0**	**26.0**	**20.0**	**16.0**
EPM7256A	100	TQFP	10.0	44.0	38.0	34.0	31.0
	144	TQFP	9.0	33.0	26.0	22.0	20.0
	208	PQFP	7.0	35.0	24.0	18.0	14.0
	256	FineLine BGA	6.2	34.0	32.0	29.0	28.0
EPM7256B	100	TQFP	10.0	44.0	38.0	34.0	31.0
		FineLine BGA	10.0	33.0	29.0	26.0	24.0
	144	TQFP	9.0	33.0	26.0	22.0	20.0
	169	Ultra FineLine BGA	14.0	38.0	36.0	34.0	30.0
	208	PQFP	7.0	35.0	24.0	18.0	14.0
	256	FineLine BGA	6.2	34.0	32.0	29.0	28.0

Table 7. Thermal Resistance of MAX 7000 Devices (Part 4 of 4) *Notes (1), (2)*

Device	Pin Count	Package	θ_{JC} (° C/W)	θ_{JA} (° C/W) Still Air	θ_{JA} (° C/W) 100 ft./min.	θ_{JA} (° C/W) 200 ft./min.	θ_{JA} (° C/W) 400 ft./min.
EPM7256E	160	PGA	**6.0**	**20.0**	**13.0**	**10.0**	**8.0**
		PQFP	**7.0**	**35.0**	**26.0**	**20.0**	**16.0**
	208	RQFP	**2.0**	**18.0**	**12.0**	**9.0**	**7.0**
EPM7256S	208	PQFP	7.0	35.0	24.0	18.0	14.0
		RQFP	**2.0**	**18.0**	**12.0**	**9.0**	**7.0**
EPM7256AE	100	TQFP	10.0	44.0	38.0	34.0	31.0
		FineLine BGA	10.0	33.0	29.0	26.0	24.0
	144	TQFP	9.0	33.0	26.0	22.0	20.0
	208	PQFP	7.0	35.0	24.0	18.0	14.0
	256	FineLine BGA	**10.3**	**33.0**	**31.0**	**29.5**	**26.6**
EPM7512AE	144	TQFP	9.0	33.0	26.0	22.0	20.0
	208	PQFP	7.0	35.0	24.0	18.0	14.0
	256	BGA	6.0	28.0	22.0	20.0	19.0
		FineLine BGA	6.5	29.6	28.4	27.0	24.2
EPM7512B	144	TQFP	9.0	33.0	26.0	22.0	20.0
	169	Ultra FineLine BGA	10.0	33.0	31.0	29.0	26.0
	208	PQFP	7.0	35.0	24.0	18.0	14.0
	256	FineLine BGA	6.5	29.6	28.4	27.0	24.2

Notes:
(1) Bold type designates measured values. Values are not measured for MAX 7000A devices.
(2) Thermal resistance values for MAX 7000A devices are preliminary.

Table 8. Thermal Resistance of MAX 5000 Devices *Note (1)*

Device	Pin Count	Package	θ_{JC} (° C/W)	θ_{JA} (° C/W)
EPM5032	28	CerDIP	**12.0**	**44.0**
		PDIP	**19.0**	**48.0**
		JLCC	**9.0**	**69.0**
		PLCC	**10.0**	**59.0**
EPM5064	44	JLCC	**15.0**	**62.0**
		PLCC	**9.0**	**52.0**
EPM5128	68	JLCC	**11.0**	**39.0**
		PLCC	**12.0**	**44.0**
		PGA	**2.0**	**32.0**
EPM5128A	68	PLCC	**12.0**	**44.0**
EPM5130	84	JLCC	**4.0**	**30.0**
		PLCC	**11.0**	**35.0**
	100	PQFP	**10.0**	**50.0**
		PGA	**4.0**	**26.0**
EPM5192	84	JLCC	**4.0**	**30.0**
		PLCC	**11.0**	**35.0**
		PGA	**2.0**	**27.0**

Note:
(1) Bold type designates measured values.

Table 9. Thermal Resistance of MAX 3000A Devices

Device	Pin Count	Package	θ_{JC} (° C/W)	θ_{JA} (° C/W) Still Air	θ_{JA} (° C/W) 100 ft./min.	θ_{JA} (° C/W) 200 ft./min.	θ_{JA} (° C/W) 400 ft./min.
EPM3032A	44	TQFP	19.0	64.0	56.0	50.0	45.0
		PLCC	9.0	52.0	45.0	41.0	36.0
EPM3064A	44	TQFP	10.0	44.0	38.0	34.0	31.0
		PLCC	11.0	35.0	23.0	18.0	14.0
	100	TQFP	10.0	44.0	38.0	34.0	31.0
EPM3128A	100	TQFP	10.0	44.0	38.0	34.0	31.0
	144	TQFP	9.0	33.0	26.0	22.0	20.0
EPM3256A	144	TQFP	9.0	33.0	26.0	22.0	20.0
	208	PQFP	7.0	35.0	24.0	18.0	14.0

Table 10. Thermal Resistance of Classic Devices *Note (1)*

Device	Pin Count	Package	θ_{JC} (° C/W)	θ_{JA} (° C/W)
EP600I	24	PDIP	22.0	67.0
		CerDIP	18.0	60.0
	28	PLCC	16.0	64.0
EP610	24	CerDIP	**10.0**	**60.0**
		PDIP	**18.0**	**55.0**
		SOIC	**17.0**	**77.0**
	28	PLCC	**13.0**	**74.0**
EP610I	24	CerDIP	**18.0**	**60.0**
		PDIP	**22.0**	**67.0**
	28	PLCC	**16.0**	**64.0**
EP900I	40	PDIP	23.0	49.0
	44	PLCC	10.0	58.0
EP910	40	CerDIP	**12.0**	**40.0**
		PDIP	**23.0**	**49.0**
	44	PLCC	**10.0**	**58.0**
EP910I	40	CerDIP	**17.0**	**44.0**
		PDIP	**29.0**	**51.0**
	44	PLCC	**16.0**	**55.0**
EP1800I	68	PLCC	13.0	44.0
EP1810	68	JLCC	**12.0**	**47.0**
		PLCC	**13.0**	**44.0**
		PGA	**6.0**	**38.0**

Table 11. Thermal Resistance of Configuration Devices (Part 1 of 2) *Note (1)*

Device	Pin Count	Package	θ_{JC} (° C/W)	θ_{JA} (° C/W)
EPC1064 EPC1064V	8	PDIP	**19**	**48**
	20	PLCC	**18**	**80**
	32	TQFP	**17**	**75**
EPC1213	8	PDIP	**19**	**48**
	20	PLCC	**18**	**80**

Table 11. Thermal Resistance of Configuration Devices (Part 2 of 2) *Note (1)*

Device	Pin Count	Package	θ_{JC} (° C/W)	θ_{JA} (° C/W)
EPC1441	8	PDIP	**19**	**48**
	20	PLCC	**18**	**80**
	32	TQFP	**17**	**75**
EPC1	8	PDIP	**16**	**70**
	20	PLCC	**18**	**80**
EPC2	20	PLCC	18	80
	32	TQFP	17	75

Note to tables:
(1) Bold type designates measured values.

Package Weights

Table 12 shows the package weights for Altera devices. The die of a device adds an insignificant amount of weight; therefore, these weights can be used for any device in that package.

Table 12. Package Weights for Altera Devices (Part 1 of 2)

Pins	Package	Weight (grams)
8	PDIP	0.5
20	PLCC	0.8
24	CerDIP	4.1
24	PDIP	1.7
24	SOIC	0.6
28	PLCC	1.1
28	PDIP	1.7
28	CerDIP	4.1
32	TQFP	0.2
40	PDIP	6.0
40	CerDIP	13.2
44	PLCC	2.3
44	JLCC	2.8
44	PQFP	0.5
44	TQFP	0.3
49	Ultra FineLine BGA	0.1
68	PGA	10.4
68	JLCC	7.1
68	PLCC	4.6
84	PLCC	6.8

Table 12. Package Weights for Altera Devices (Part 2 of 2)

Pins	Package	Weight (grams)
84	JLCC	10.9
84	PGA	10.6
100	PQFP	1.6
100	PGA	14.2
100	TQFP	0.5
100	FineLine BGA	0.2
144	TQFP	1.3
160	PQFP	5.4
160	PGA	19.9
169	Ultra FineLine BGA	0.3
192	PGA	24.1
196	FineLine BGA	0.3
208	PQFP	5.7
208	RQFP	10.8
225	BGA	2.1
232	PGA	25.5
240	RQFP	15.1
240	PQFP	7.0
256	BGA	2.1
256	FineLine BGA	0.4
280	PGA	29.5
304	RQFP	26.3
324	FineLine BGA	0.6
356	BGA	7.0
403	PGA	29.5
484	FineLine BGA	0.7
503	PGA	59.0
599	PGA	69.0
600	BGA	12.0
652	BGA	14.9
655	PGA	74.9
672	FineLine BGA	1.2
984	PGA	*(1)*
1,020	FineLine BGA	*(1)*

Note:
(1) For package weight information, contact Altera Applications.

Package Outlines

Package outlines are listed in order of ascending pin count. Altera package outlines meet the requirements of ***JEDEC Publication No. 95***. Table 13 lists the JEDEC package outlines that are used with Altera devices.

Table 13. JEDEC Package Outline Cross Reference (Part 1 of 2) *Note (1)*

Pins	Package	JEDEC Outline
8	PDIP	MS-001
20	PLCC	MS-018
24	CerDIP	MO-036
24	PDIP	MS-001
24	SOIC	MS-013
28	SOIC	MS-013
28	PLCC	MS-018
28	JLCC	MO-087
28	PDIP	MS-001
28	CerDIP	MO-058
32	TQFP	MO-136
40	PDIP	MS-011
40	CerDIP	MS-103
44	PLCC	MS-018
44	JLCC	MO-087
44	PQFP	MO-108
44	TQFP	MO-136
49	Ultra FineLine BGA	*(1)*
68	PGA	MO-067
68	JLCC	MO-087
68	PLCC	MS-018
84	JLCC	MO-087
84	PLCC	MS-018
84	PGA	MO-067
100	PQFP	MO-108
100	TQFP	MO-136
100	PGA	MO-067
100	FineLine BGA	MO-192
144	TQFP	MO-136
160	PQFP	MO-108
160	PGA	MO-067
169	Ultra FineLine BGA	*(1)*

Table 13. JEDEC Package Outline Cross Reference (Part 2 of 2) *Note (1)*

Pins	Package	JEDEC Outline
192	PGA	MO-067
196	FineLine BGA	MO-192
208	PQFP	MO-143
208	RQFP	MO-143
225	BGA	MO-151
232	PGA	MO-067
240	RQFP	MO-143
240	PQFP	MO-143
256	BGA	MO-151
256	FineLine BGA	MO-192
280	PGA	MO-067
304	RQFP	MO-143
324	FineLine BGA	MO-192
356	BGA	MO-192
403	PGA	–
484	FineLine BGA	MO-192 *(2)*
503	PGA	–
599	PGA	–
600	BGA	MO-192
652	BGA	MO-192
655	PGA	–
672	FineLine BGA	MO-192 *(2)*
672	Flip Chip	–
984	PGA	–
1,020	FineLine BGA	–

Notes:
(1) For more information, contact Altera Applications at (800) 800-EPLD.
(2) These packages exceed the JEDEC "A" dimension in height.

Table 14 shows the different packages and pin counts for Altera devices.

Table 14. Packages & Pin Counts (Part 1 of 2)

Package	Code	Pin Count
BGA	B	225
		256
		356
		600
		652
FineLine BGA	F	100
		196
		256
		324
		484
		672
		1,020
Ultra FineLine BGA	U	49
		169
CerDIP	D	24
		40
PGA	G	68
		84
		100
		160
		192
		232
		280
		403
		503
		599
		655
		984
JLCC	J	28
		44
		68
		84

Table 14. Packages & Pin Counts (Part 2 of 2)

Package	Code	Pin Count
PLCC	L	20
		28
		44
		68
		84
PDIP	P	8
		24
		40
PQFP	Q	44
		100
		160
		208
		240
RQFP	R	208
		240
		304
SOIC	S	24
TQFP	T	32
		44
		100
		144

Table 15 summarizes the maximum lead coplanarity for Altera J-lead and QFP packages.

Table 15. Maximum Lead Coplanarity for J-Lead, PLCC, BGA, FineLine BGA & QFP Packages

Package	Maximum Lead Coplanarity
JLCC	0.006 inches (0.15 mm)
PLCC	0.004 inches (0.10 mm)
QFP packages with a lead pitch of 0.65 mm or greater	0.004 inches (0.10 mm)
QFP packages with a lead pitch of 0.5 mm	0.003 inches (0.08 mm)
QFP packages with 208 pins or greater	0.003 inches (0.08 mm)
BGA	0.008 inches (0.20 mm)
FineLine BGA	0.008 inches (0.20 mm)

For information on device package ordering codes, see *Ordering Information* in this data book.

Dimension Formats

Package outline dimensions are shown in the following formats:

min. inches (min. millimeters)
max. inches (max. millimeters)

or:

nominal inches ± tolerance
(nominal millimeters ± tolerance)

or:

inches
(millimeters) BSC, Min., Max., Ref., Typ., R, Dia., Sq.

Table 16 shows the units used to describe package outline dimensions.

Table 16. Package Outline Units

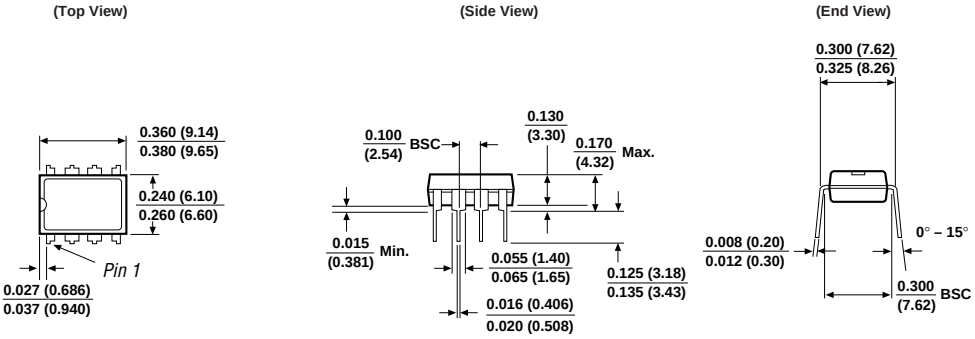
Unit	Description
BSC	Basic. Represents theoretical exact dimension or dimension target.
Min.	Minimum dimension specified.
Max.	Maximum dimension specified.
Ref.	Reference. Represents dimension for reference use only. This value is not a device specification.
Typ.	Typical. Provided as a general value. This value is not a device specification.
R	Radius. Represents curve dimension.
Dia.	Diameter. Represents curve dimension.
Sq.	Square. Indicates a square feature for a package with equal length and width dimensions.

The following figures show the package outlines for all Altera devices.

Controlling dimensions are noted on package outline drawings. The 984-pin PGA and the 1,020-pin FineLine BGA package outline drawings will be available in future revisions of this document.

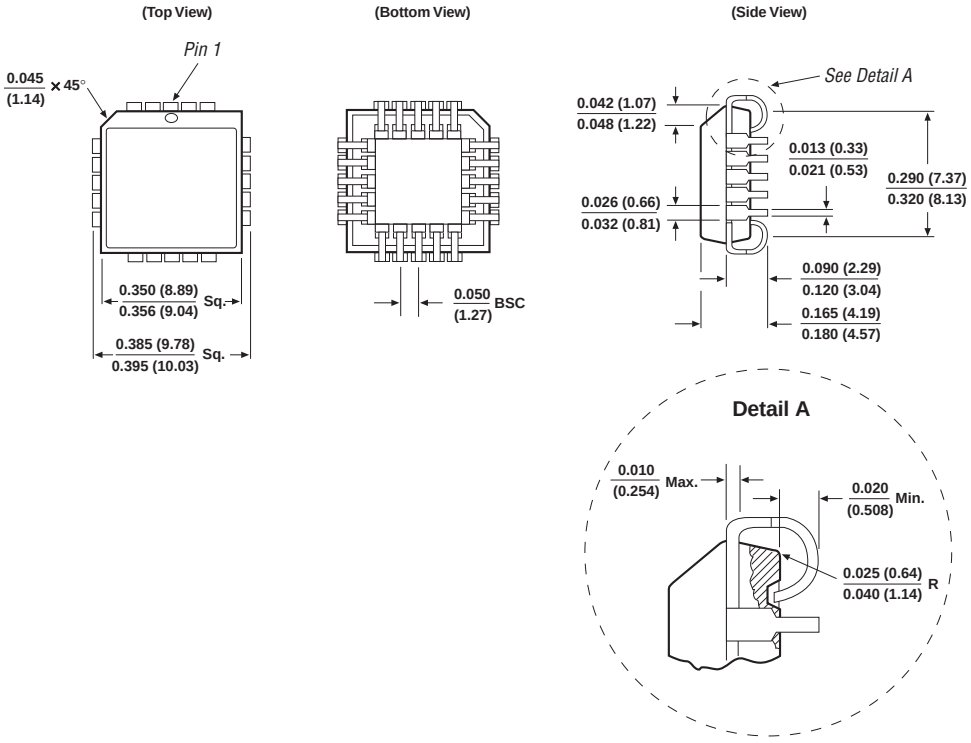
8-Pin Plastic Dual In-Line Package (PDIP)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



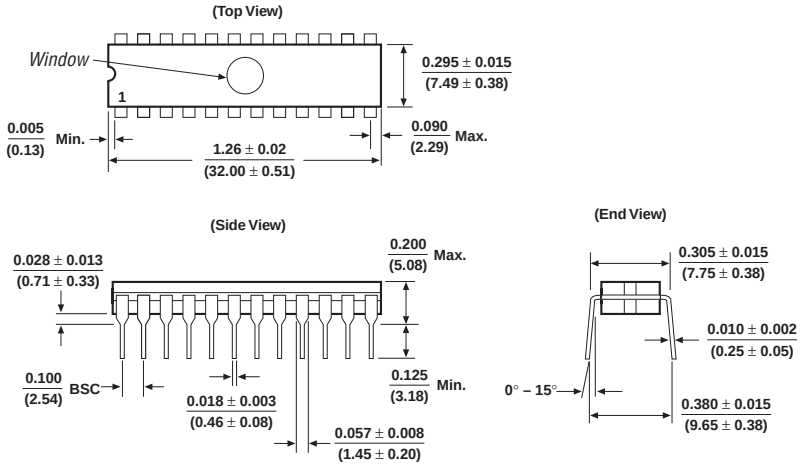
20-Pin Plastic J-Lead Chip Carrier (PLCC)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



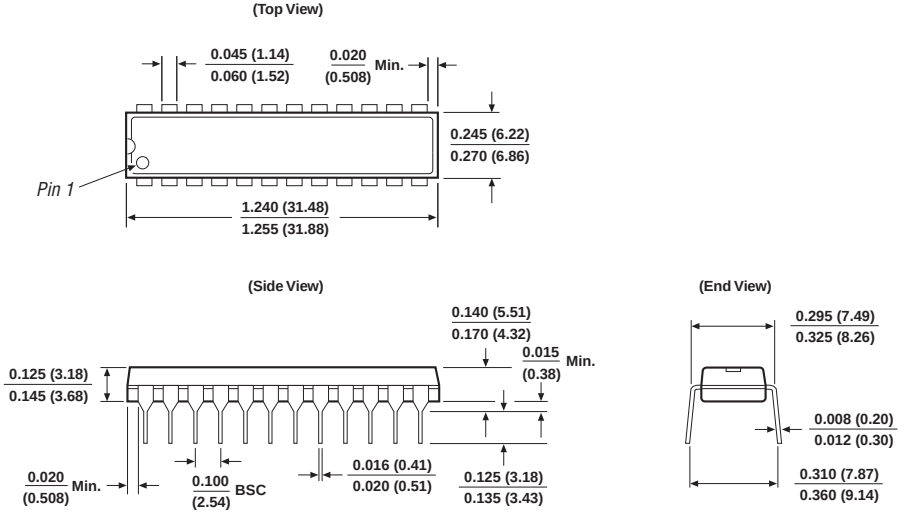
24-Pin Ceramic Dual In-Line Package (CerDIP)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



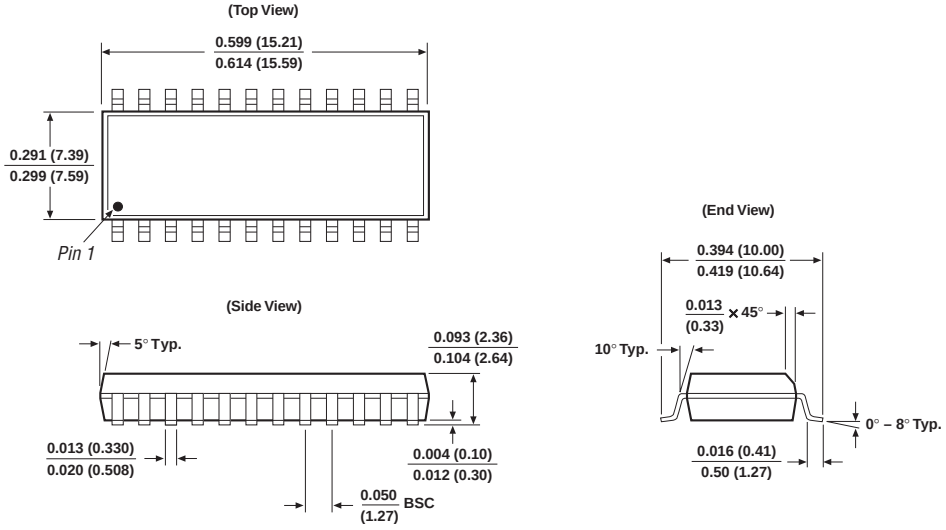
24-Pin Plastic Dual In-Line Package (PDIP)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



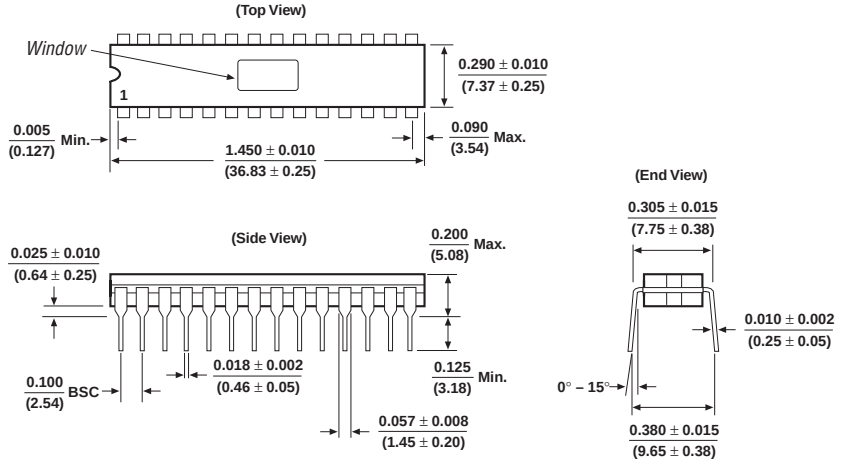
24-Pin Plastic Small-Outline Integrated Circuit (SOIC)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



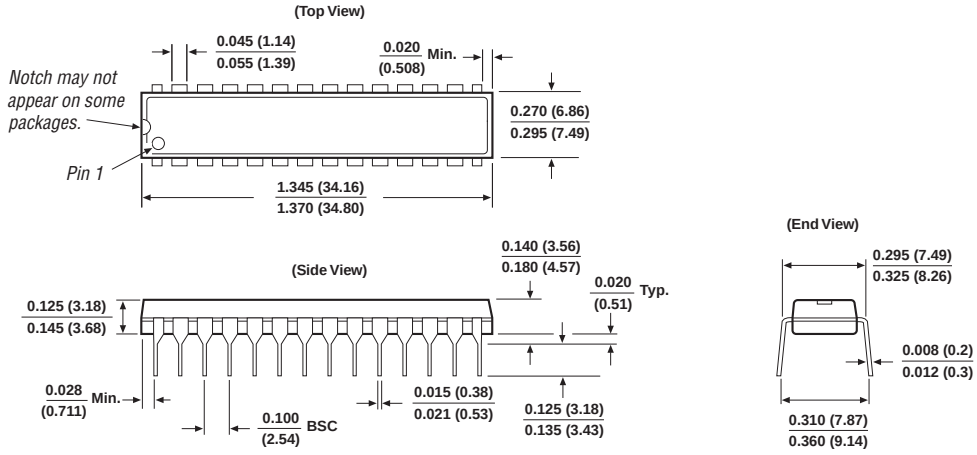
28-Pin Ceramic Dual In-Line Package (CerDIP)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



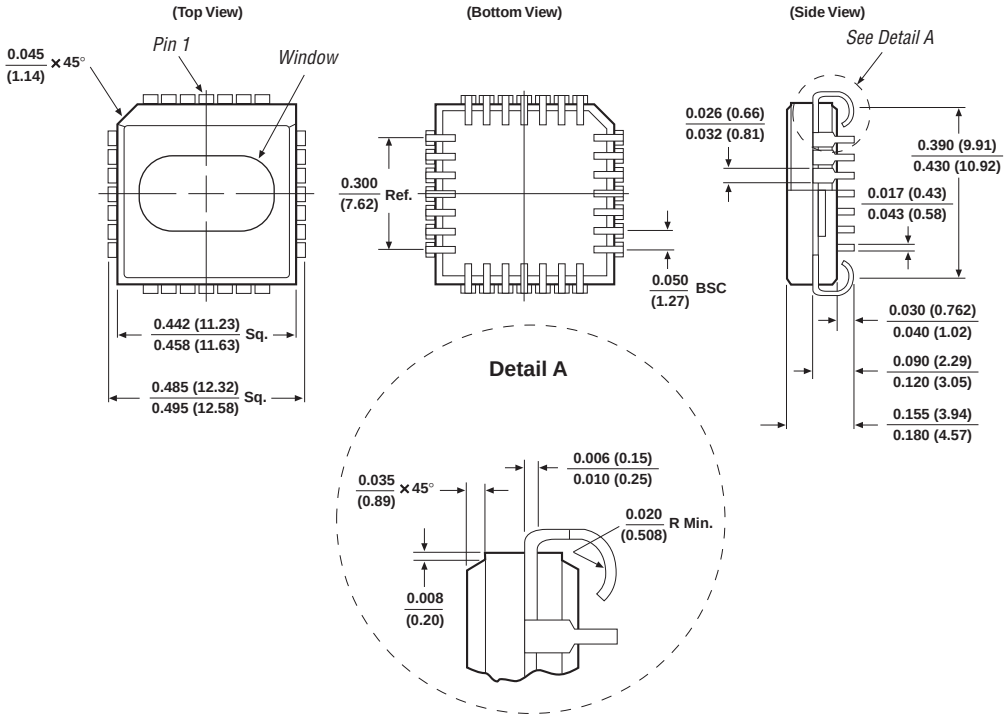
28-Pin Plastic Dual In-Line Package (PDIP)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



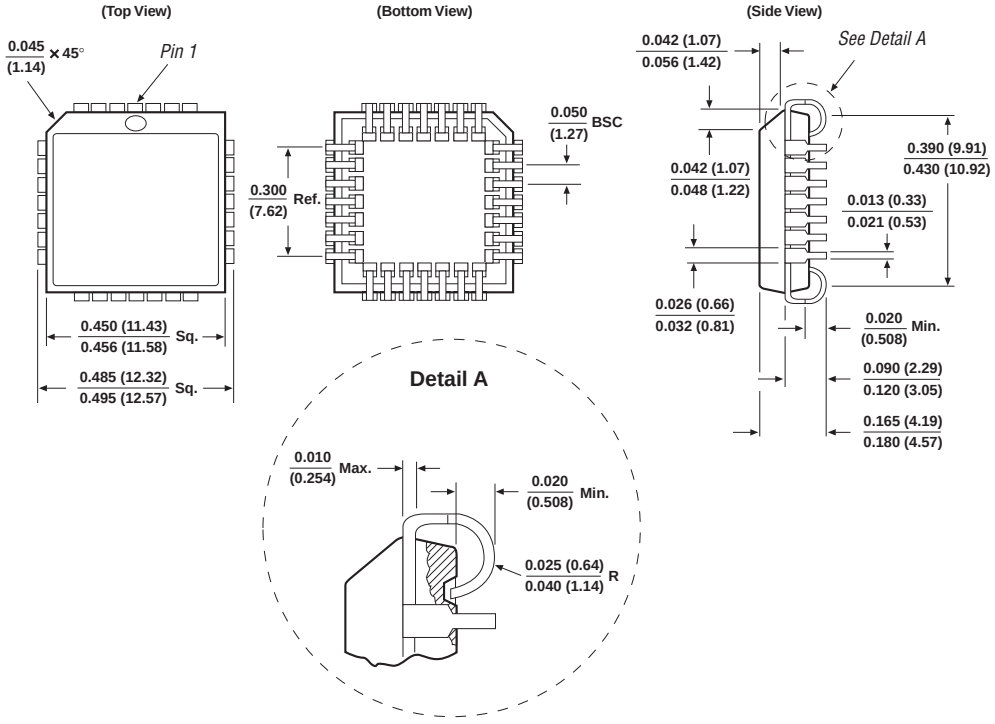
28-Pin Ceramic J-Lead Chip Carrier (JLCC)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



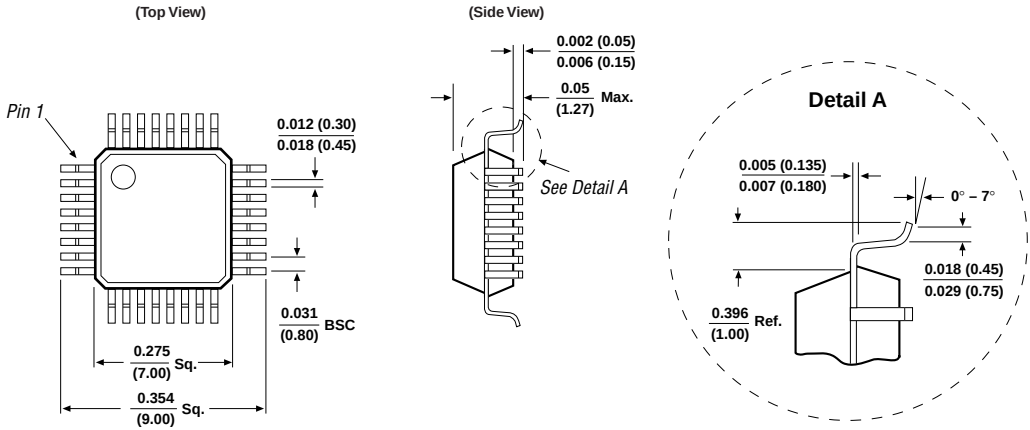
28-Pin Plastic J-Lead Chip Carrier (PLCC)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



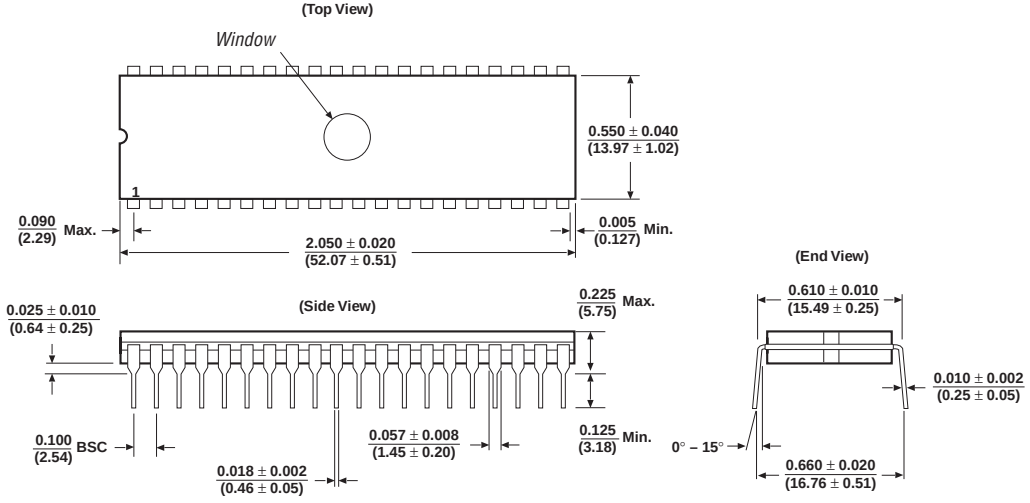
32-Pin Plastic Thin Quad Flat Pack (TQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



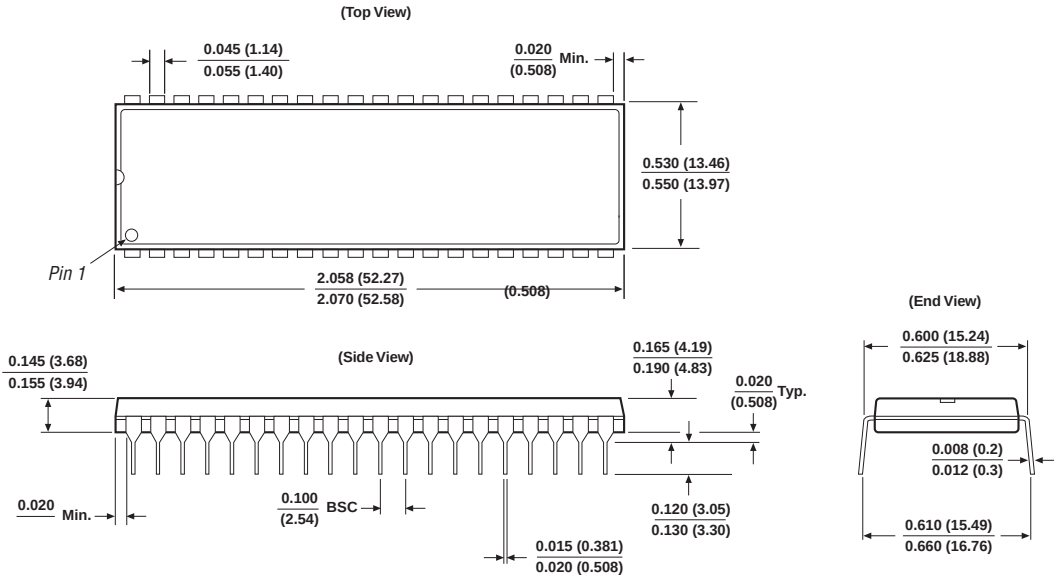
40-Pin Ceramic Dual In-Line Package (CerDIP)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



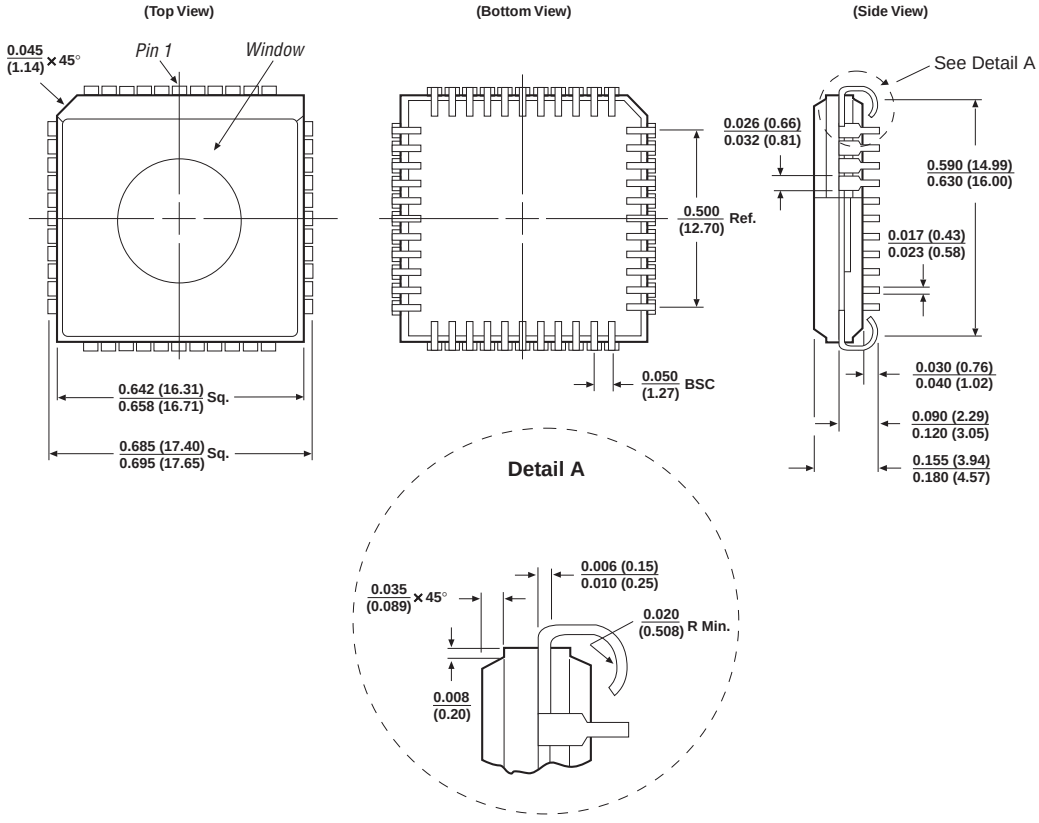
40-Pin Plastic Dual In-Line Package (PDIP)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



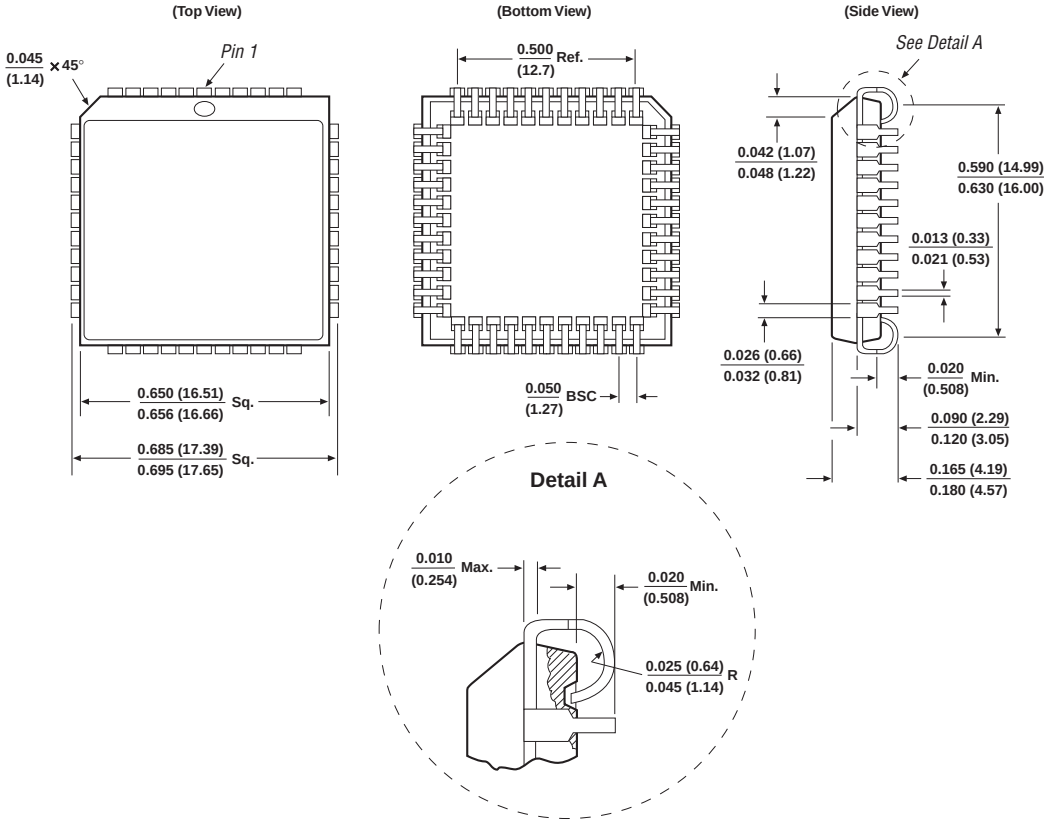
44-Pin Ceramic J-Lead Chip Carrier (JLCC)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



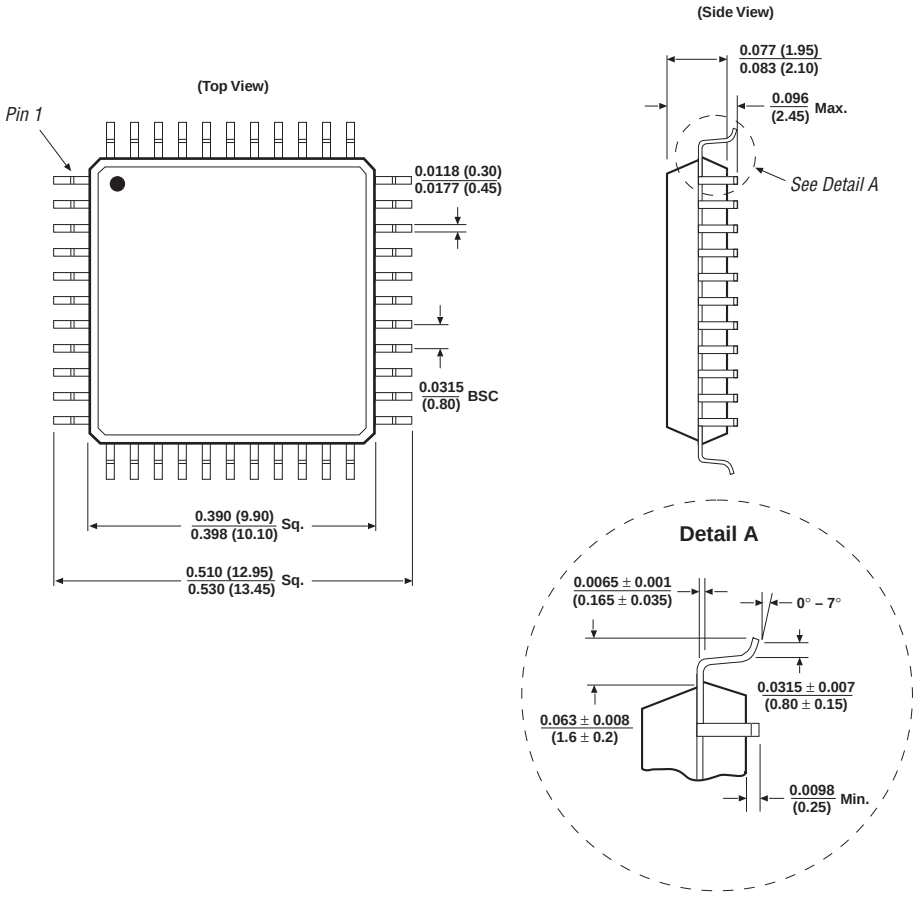
44-Pin Plastic J-Lead Chip Carrier (PLCC)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



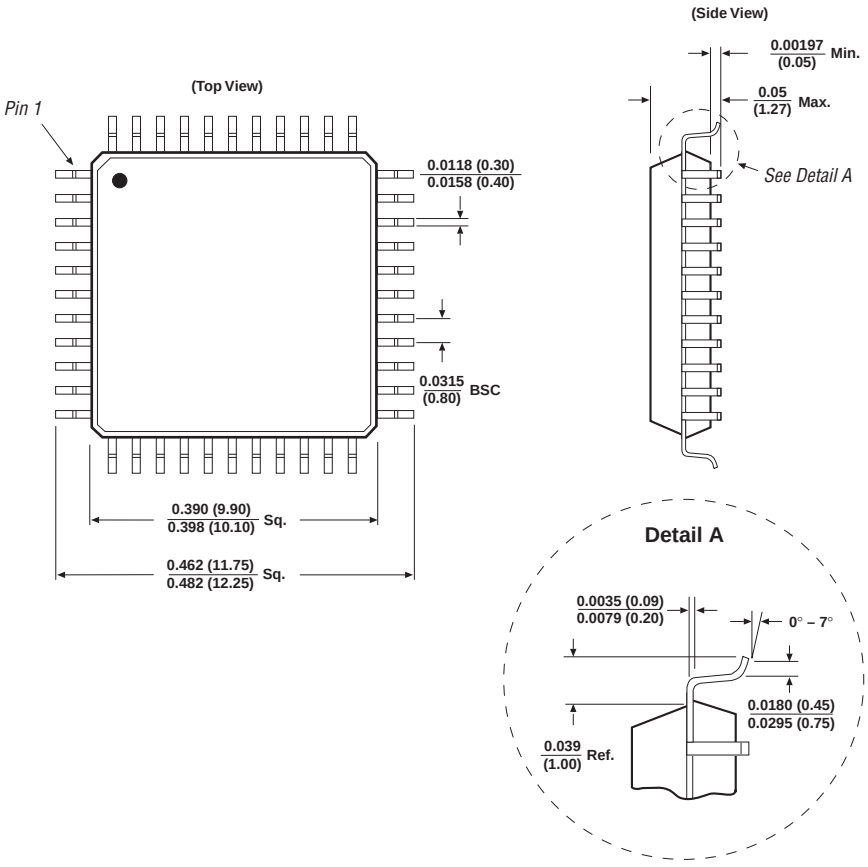
44-Pin Plastic Quad Flat Pack (PQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



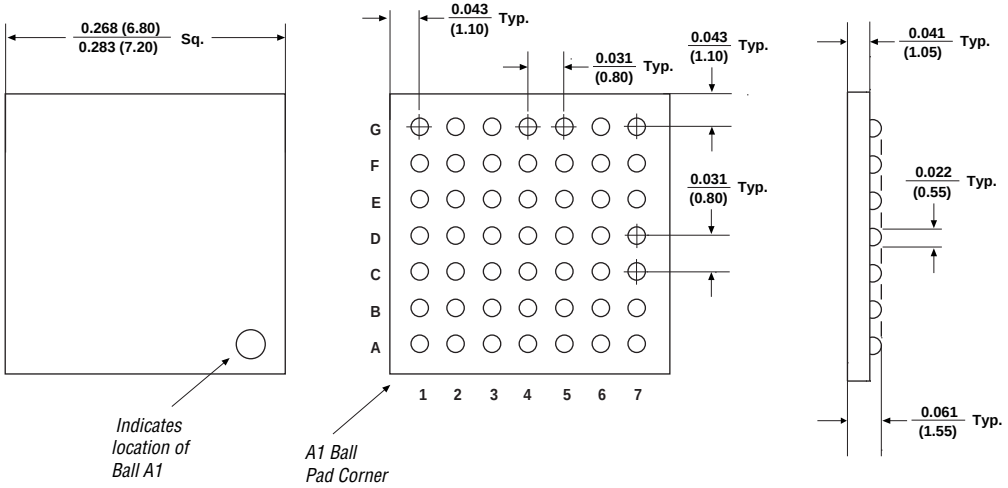
44-Pin Plastic Thin Quad Flat Pack (TQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



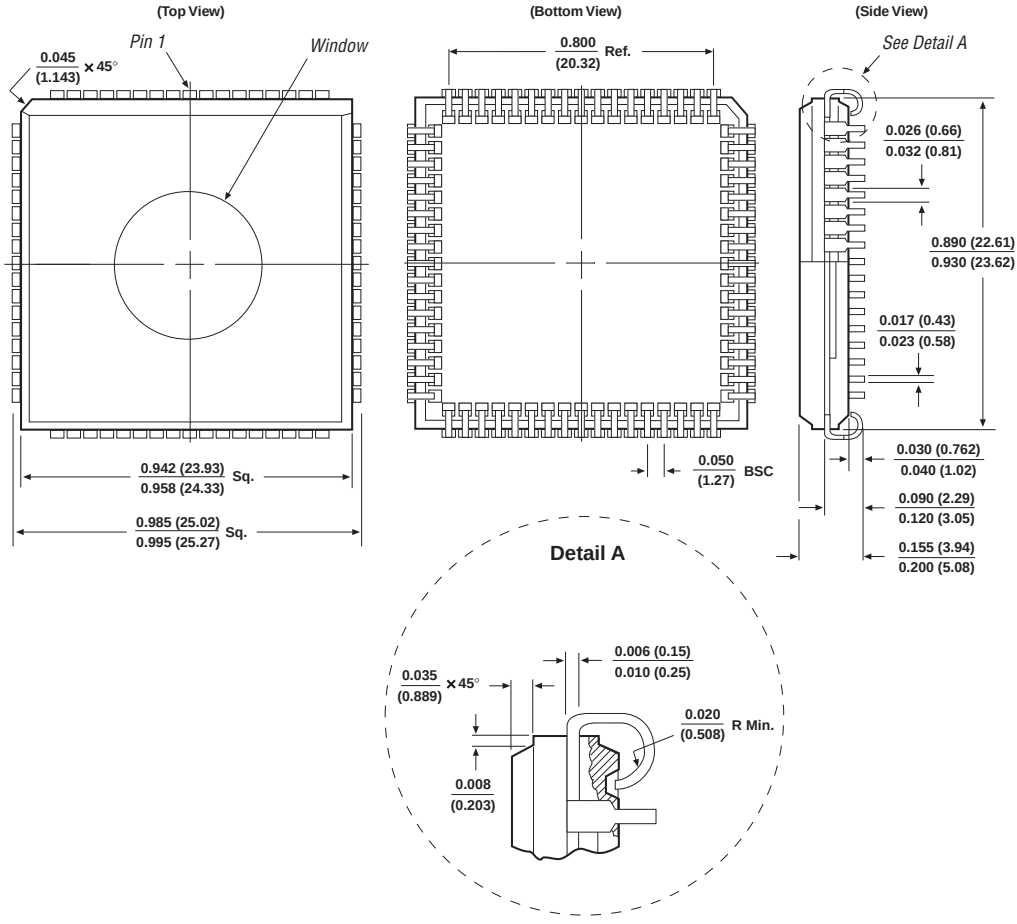
49-Ultra FineLine BGA

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



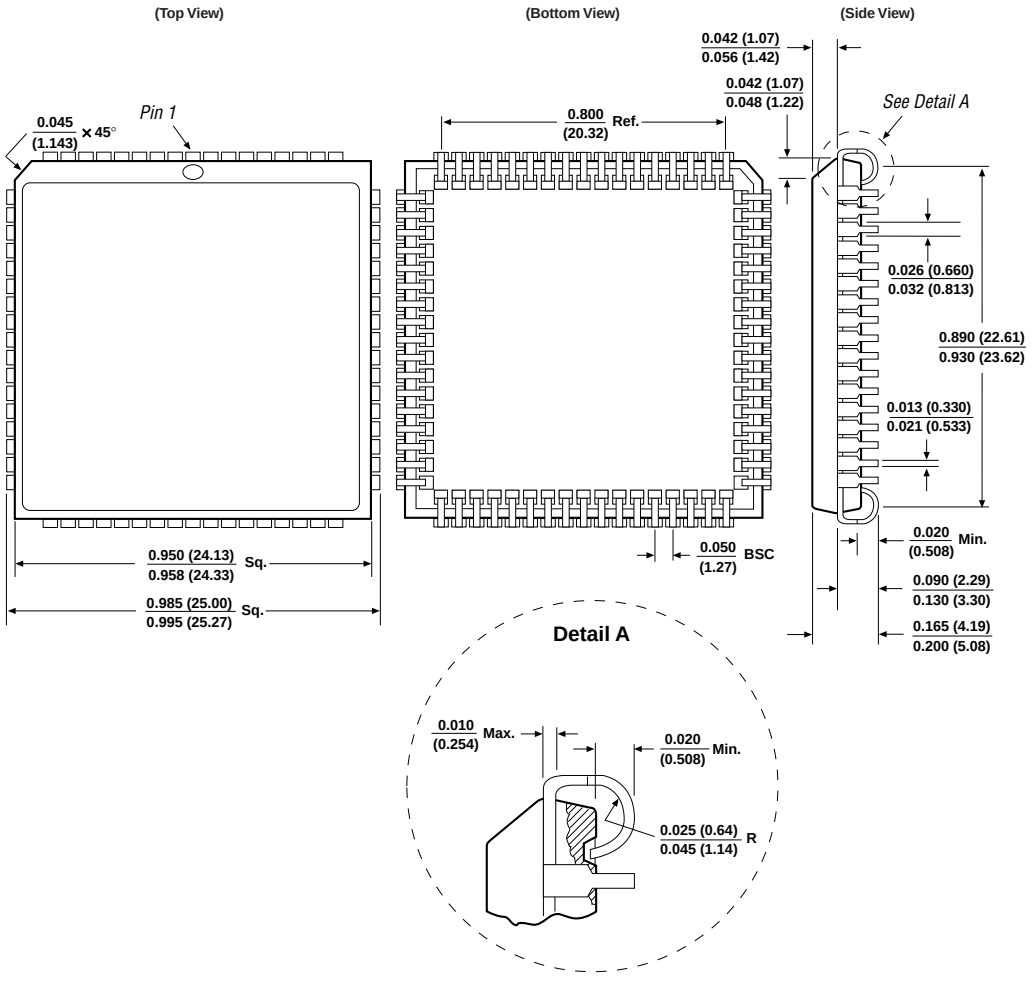
68-Pin Ceramic J-Lead Chip Carrier (JLCC)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



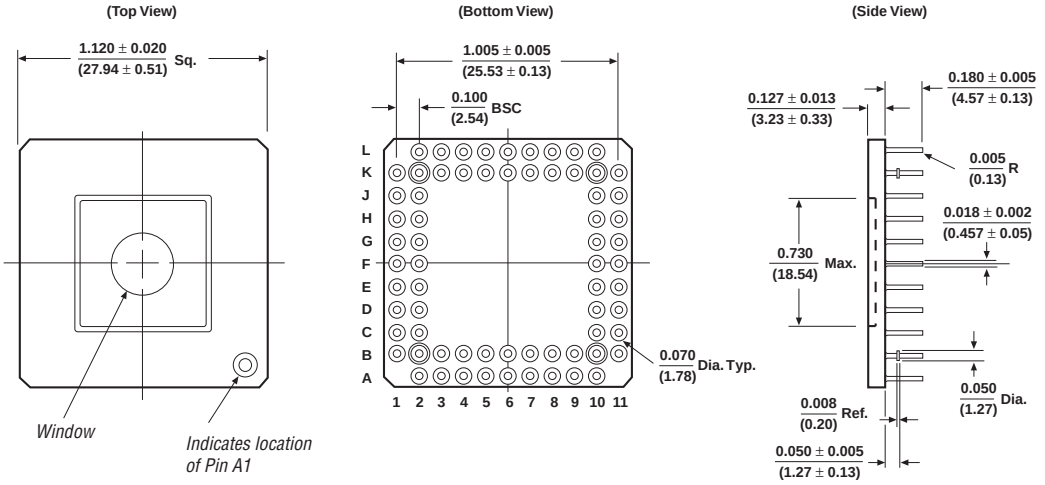
68-Pin Plastic J-Lead Chip Carrier (PLCC)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



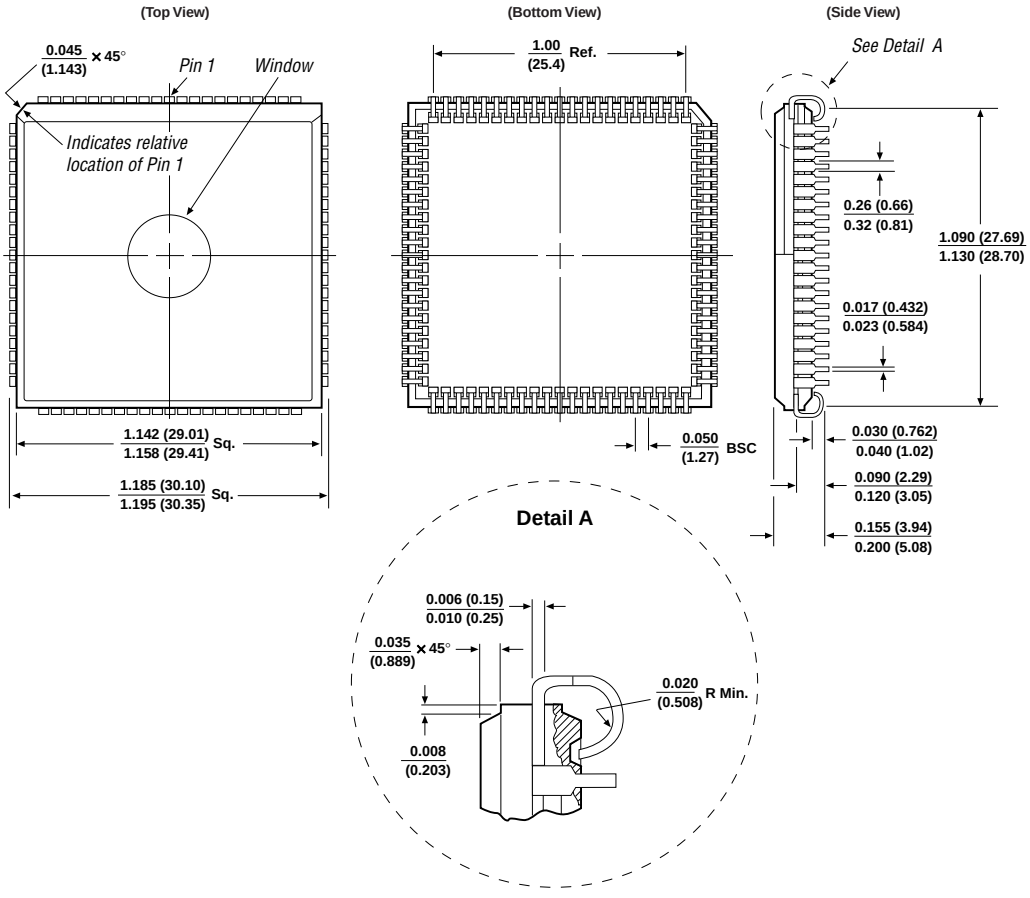
68-Pin Small Outline Ceramic Pin-Grid Array (PGA)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



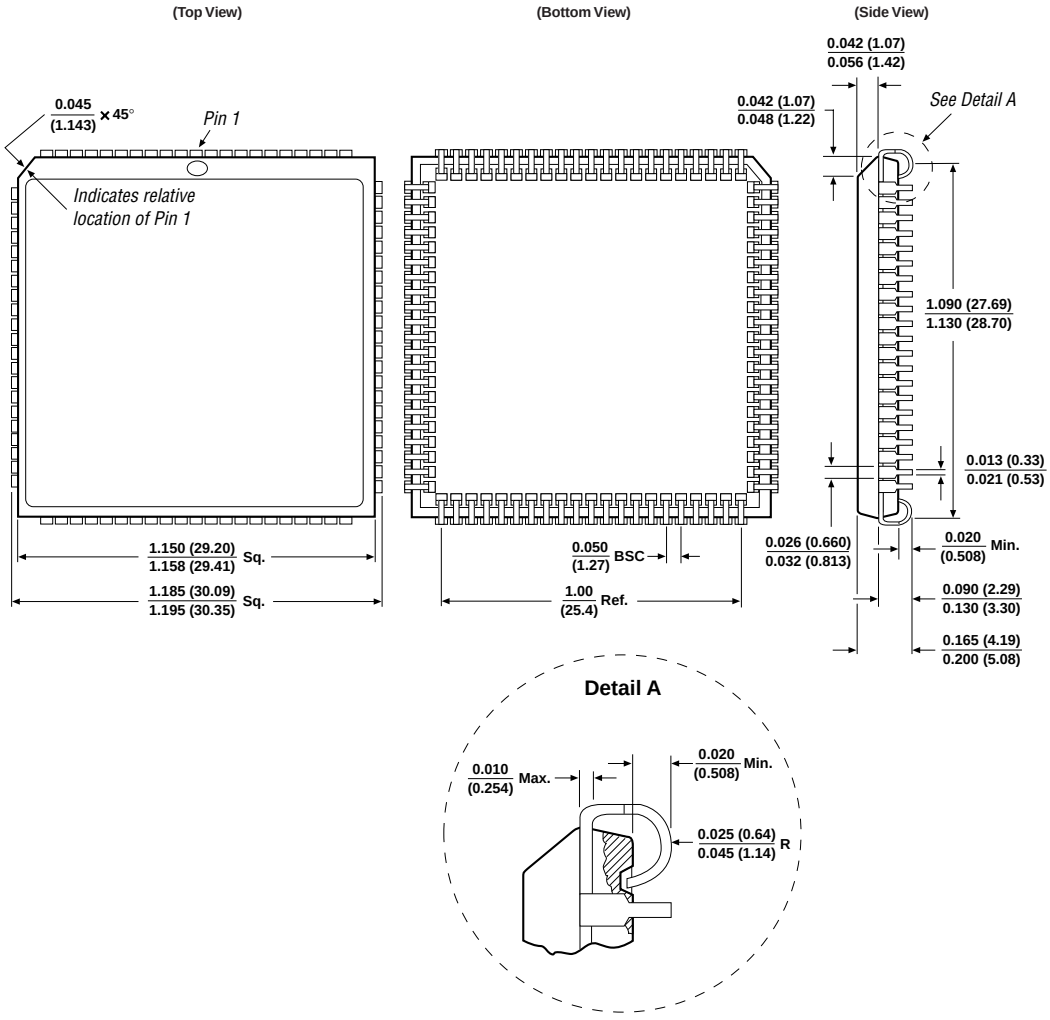
84-Pin Ceramic J-Lead Chip Carrier (JLCC)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



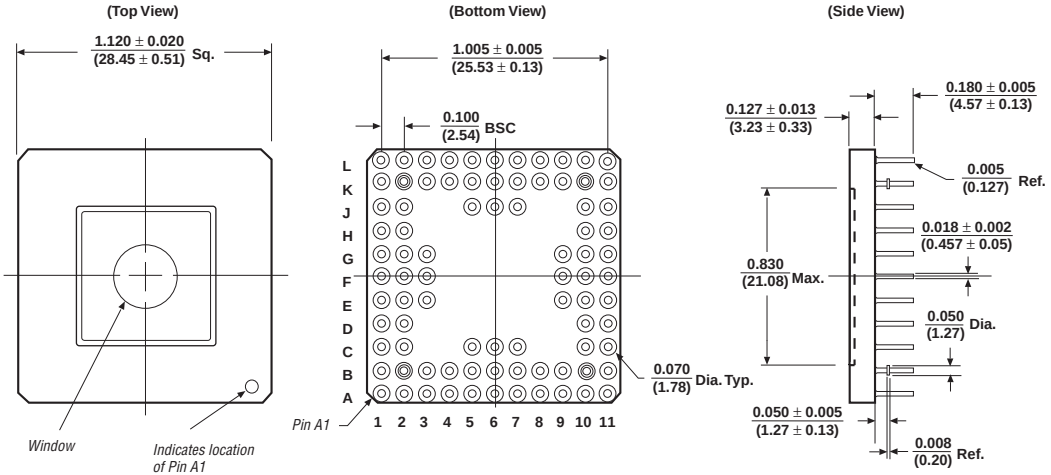
84-Pin Plastic J-Lead Chip Carrier (PLCC)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



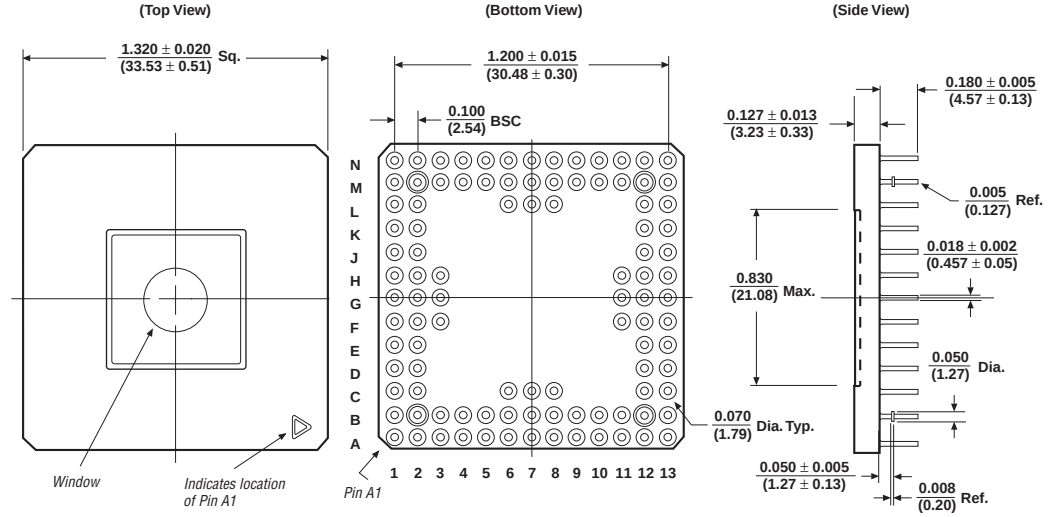
84-Pin Ceramic Pin-Grid Array (PGA)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



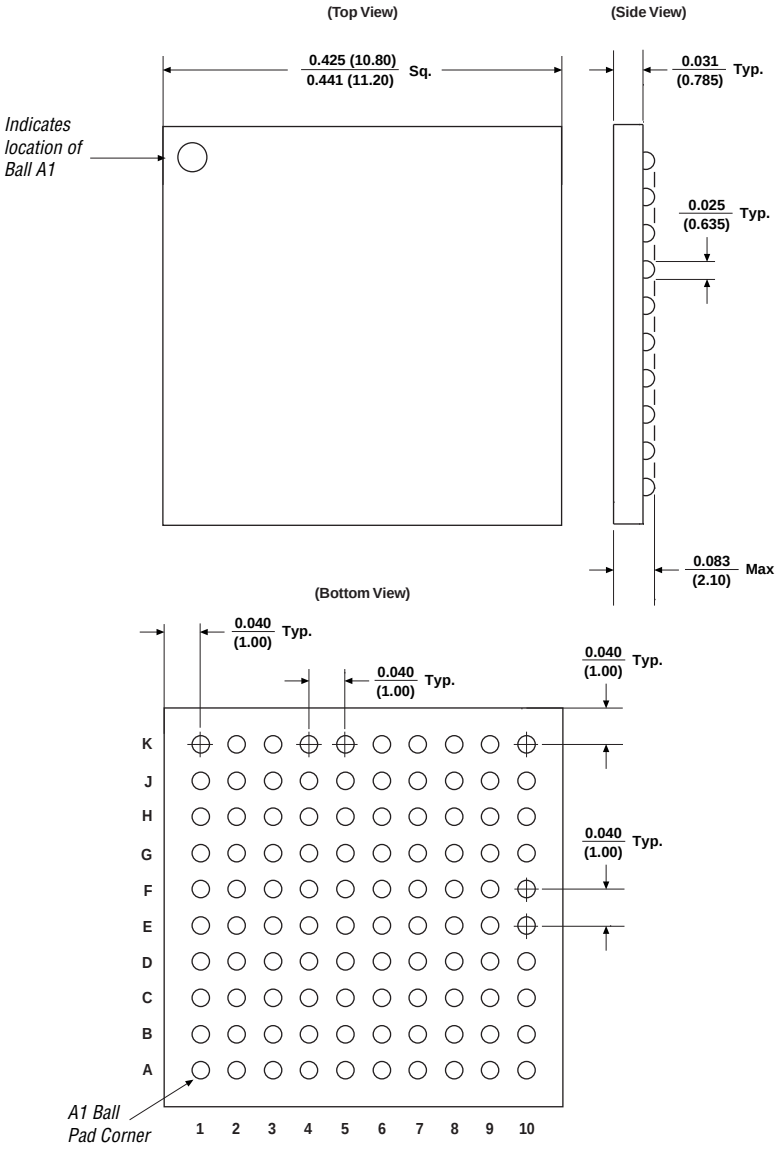
100-Pin Ceramic Pin-Grid Array (PGA)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



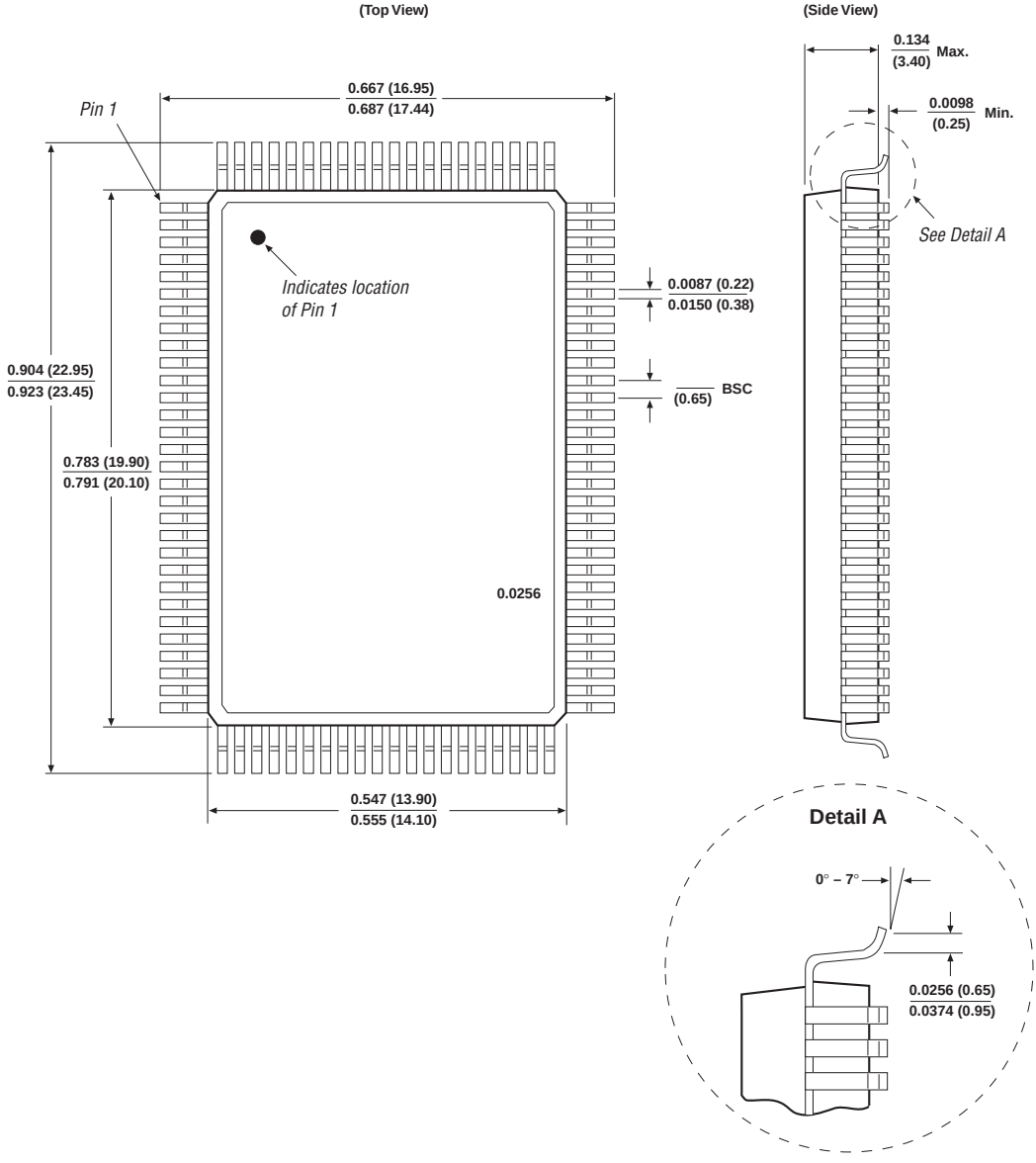
100-Pin FineLine BGA

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



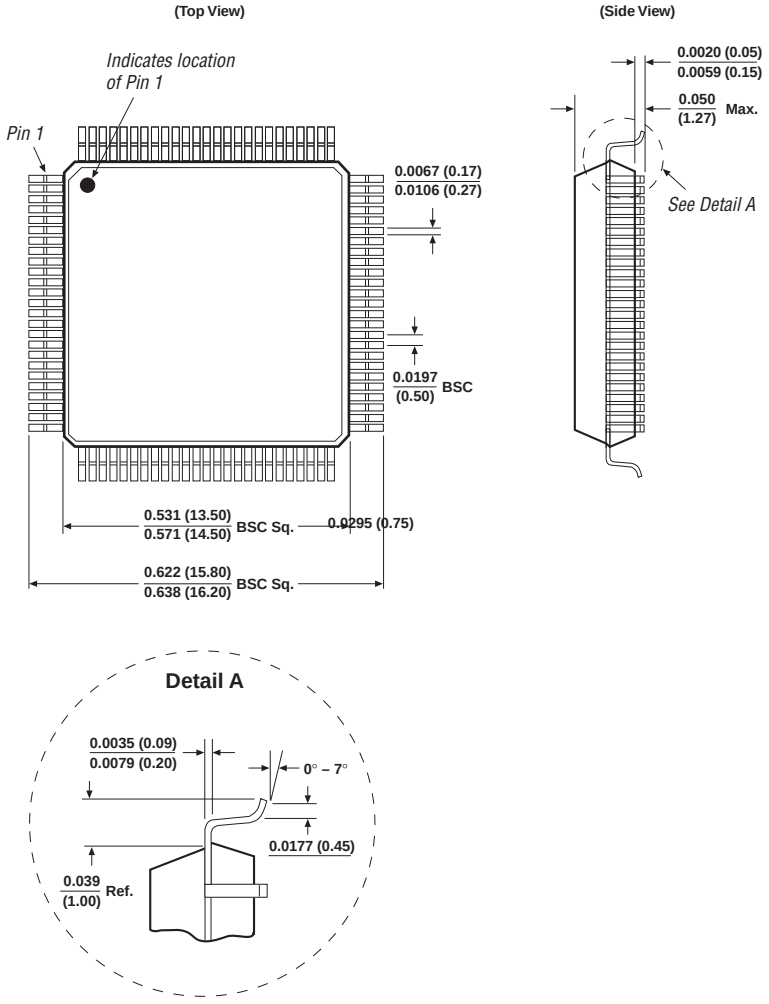
100-Pin Plastic Quad Flat Pack (PQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



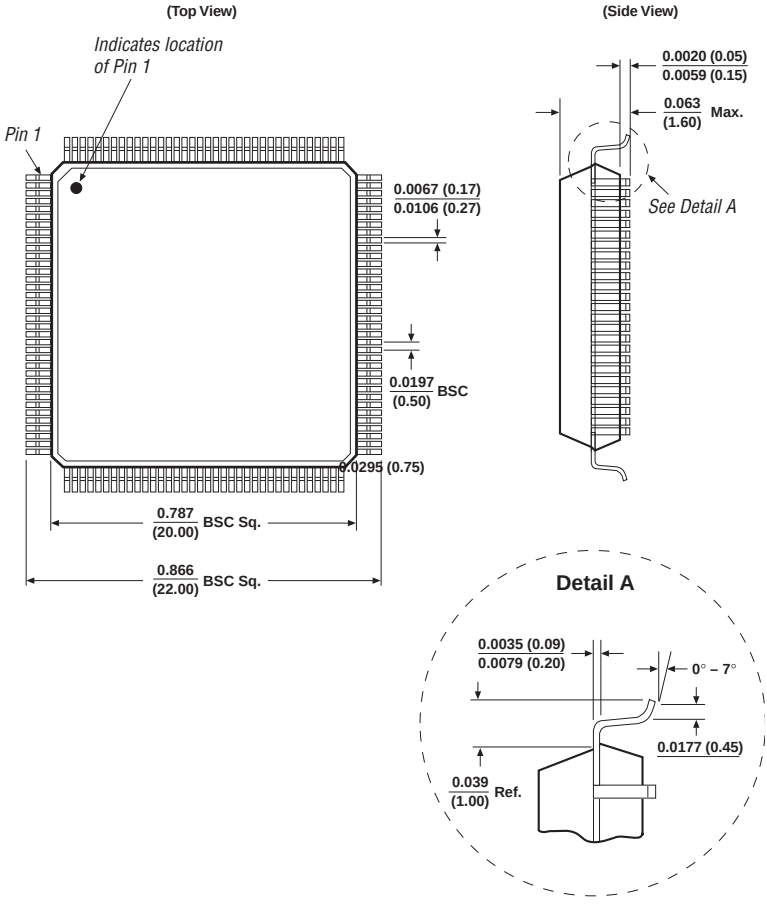
100-Pin Plastic Thin Quad Flat Pack (TQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



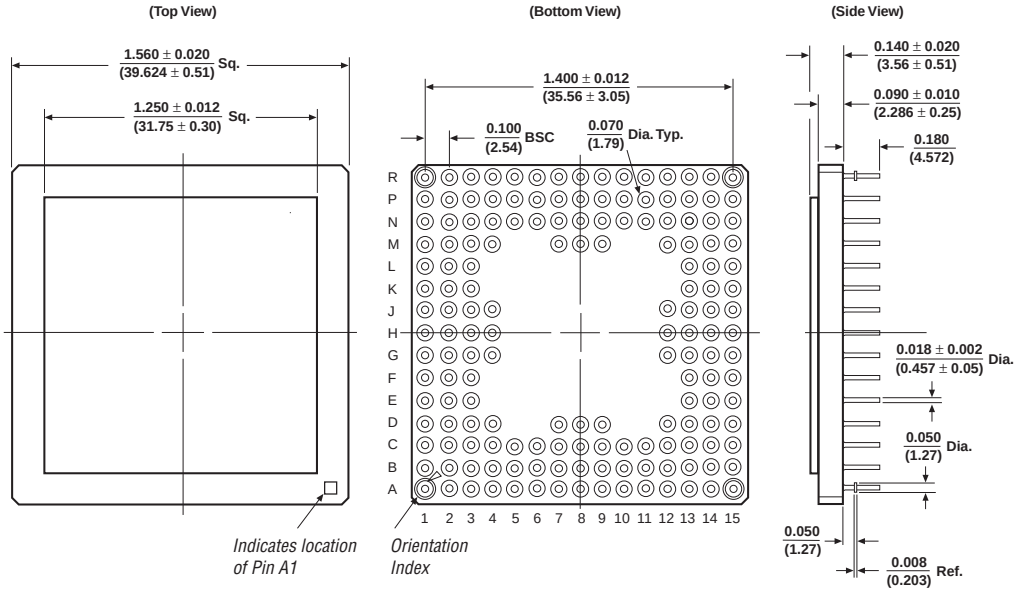
144-Pin Plastic Thin Quad Flat Pack (TQFP)

Controlling measurement is in millimeters, shown in parenthesis. Inch measurements are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



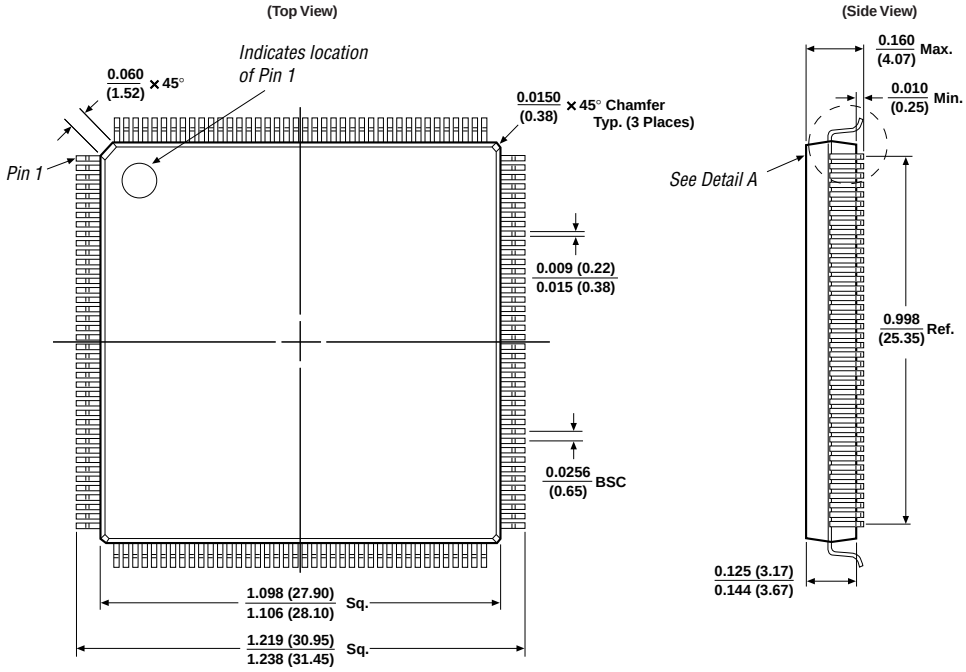
160-Pin Ceramic Pin-Grid Array (PGA)

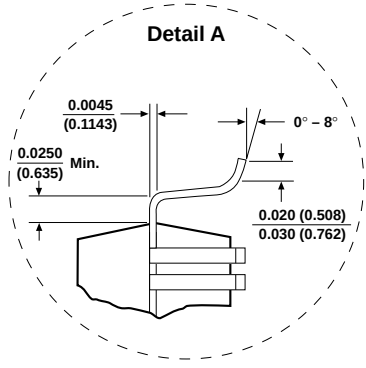
Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



160-Pin Plastic Quad Flat Pack (PQFP)

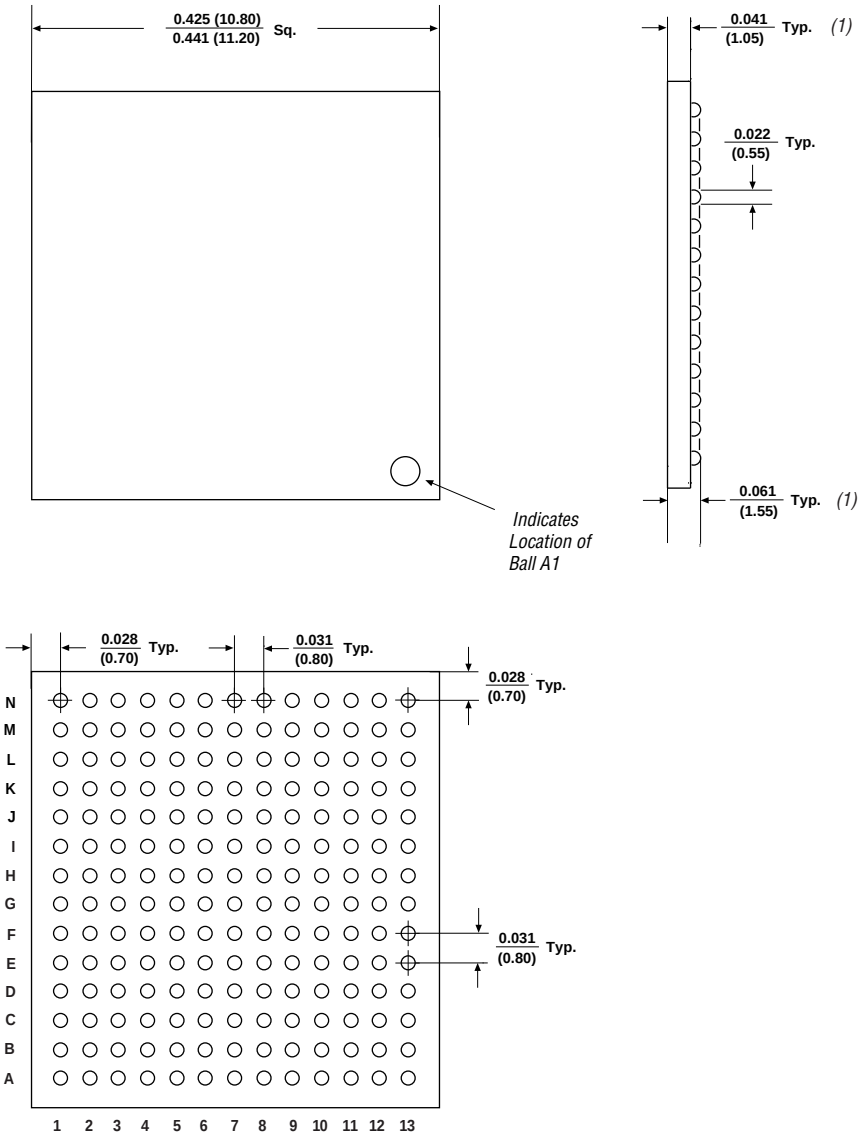
Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.





169-Pin Ultra FineLine BGA

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.

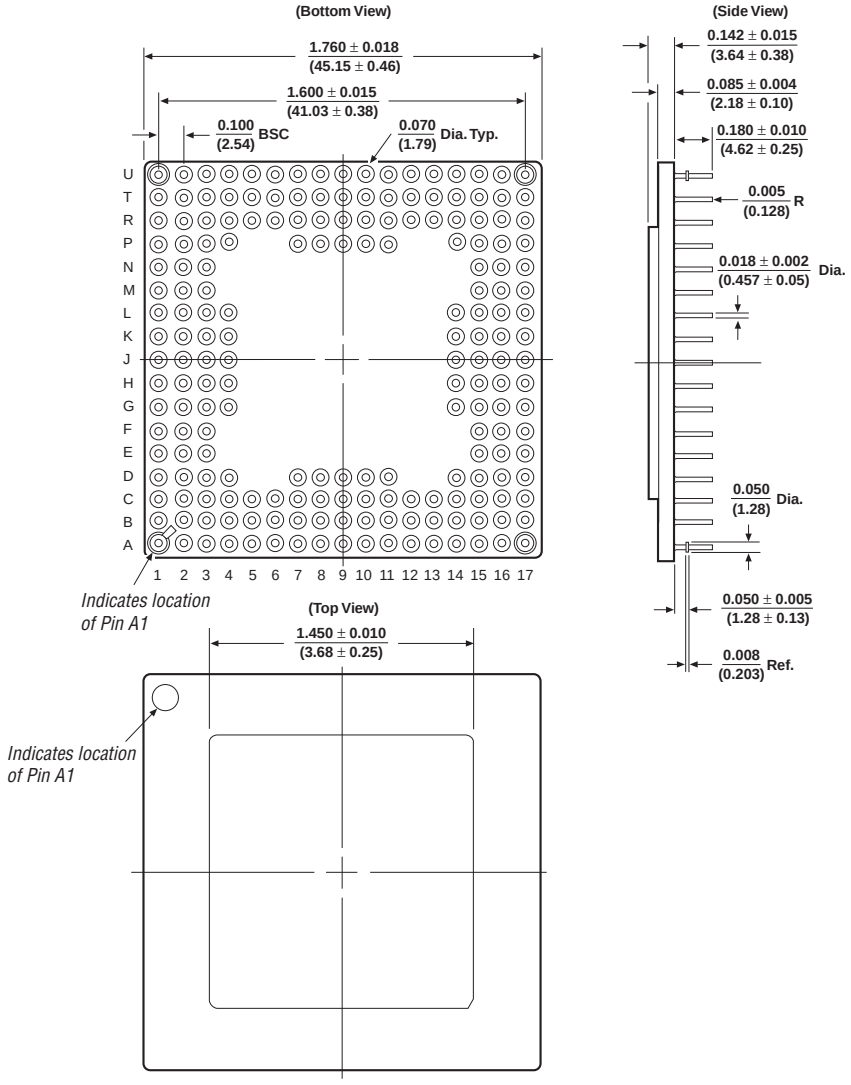


Note:

(1) The EPM7512B uses a thicker version of this package. Package thickness of this EPM7512B device is 1.6 mm typical and total package height is 2.2 mm maximum.

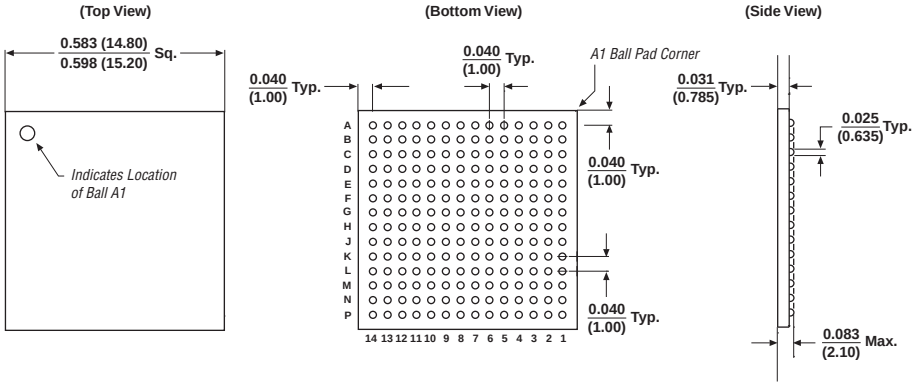
192-Pin Ceramic Pin-Grid Array (PGA)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



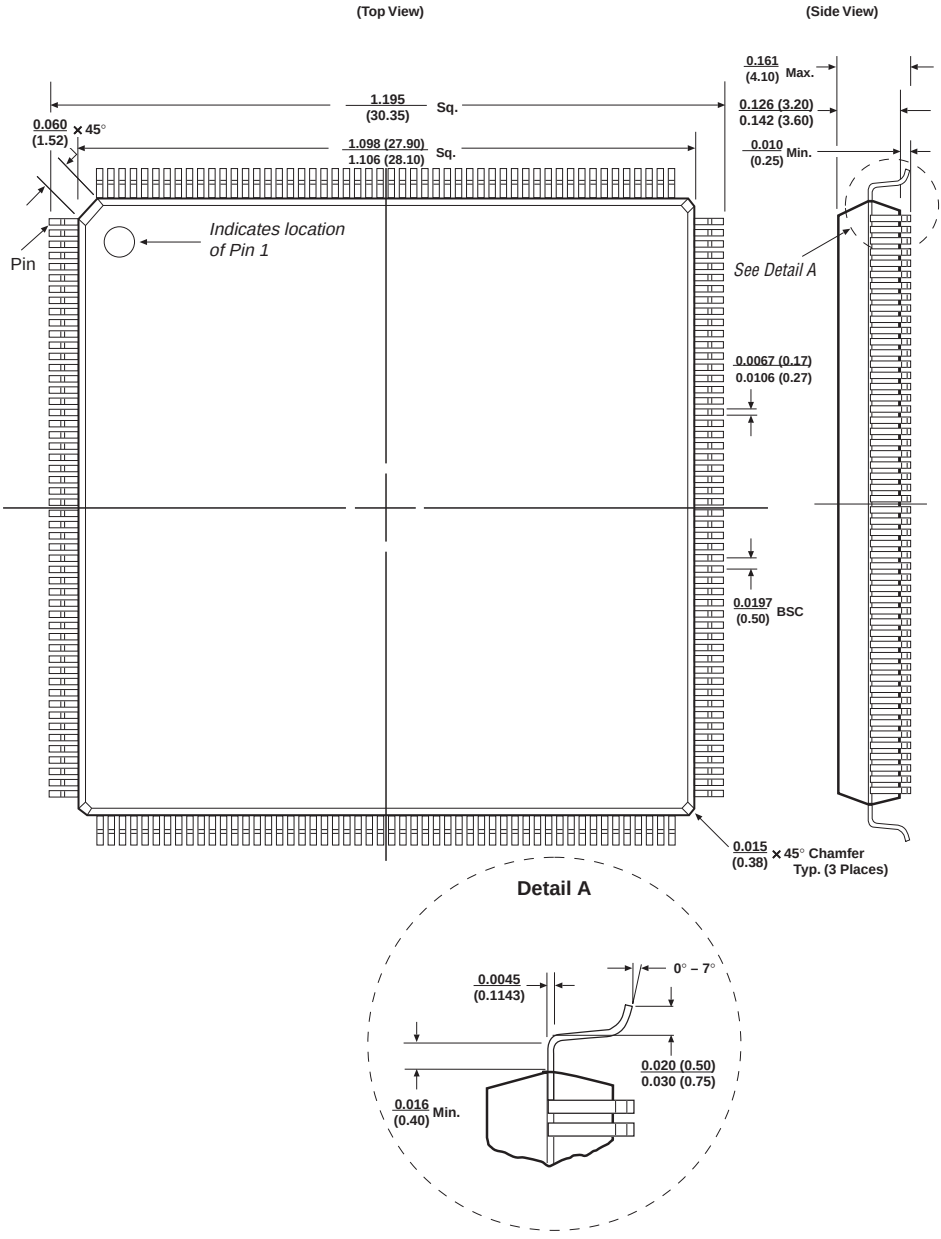
196-Pin FineLine BGA

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



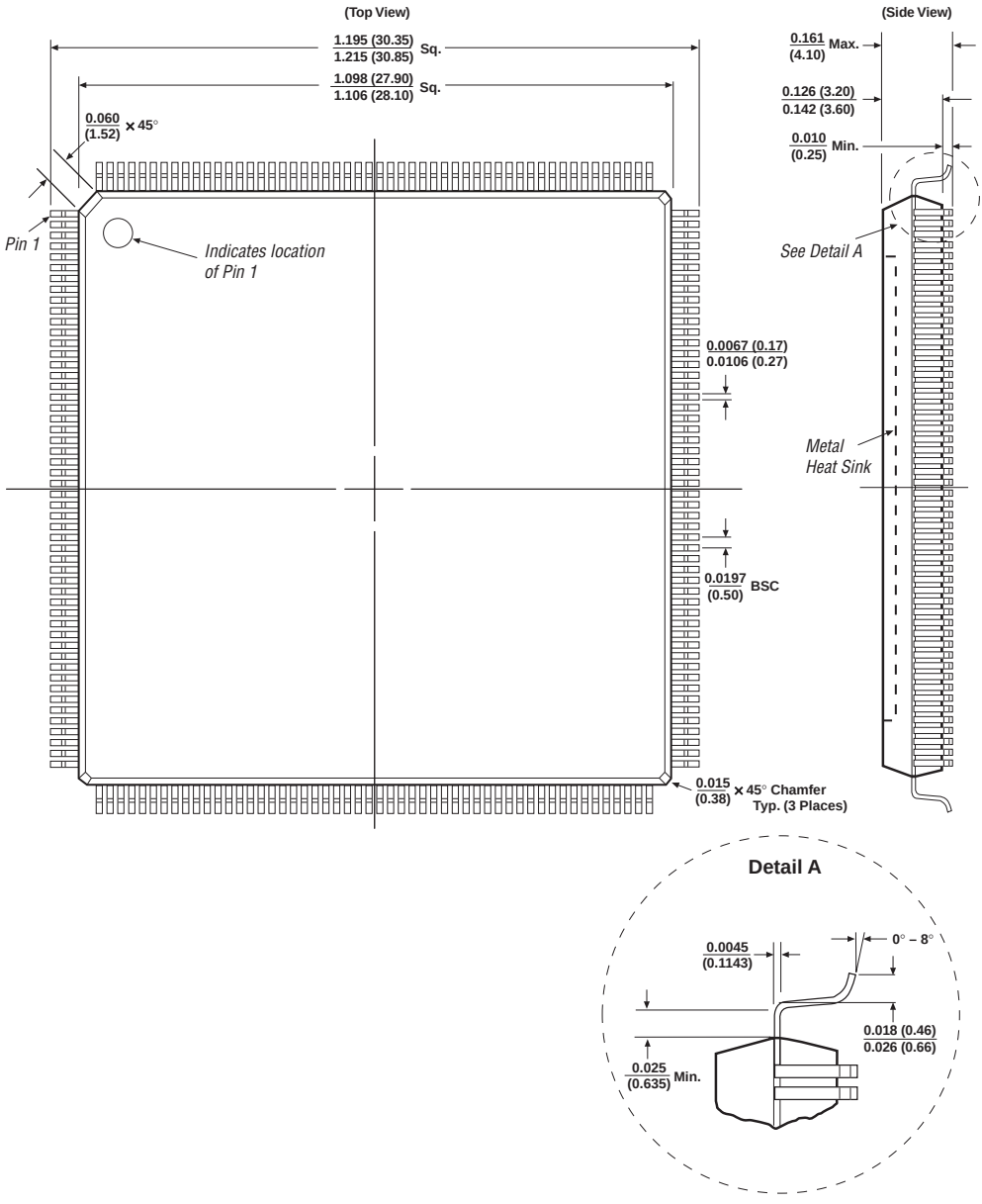
208-Pin Plastic Quad Flat Pack (PQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



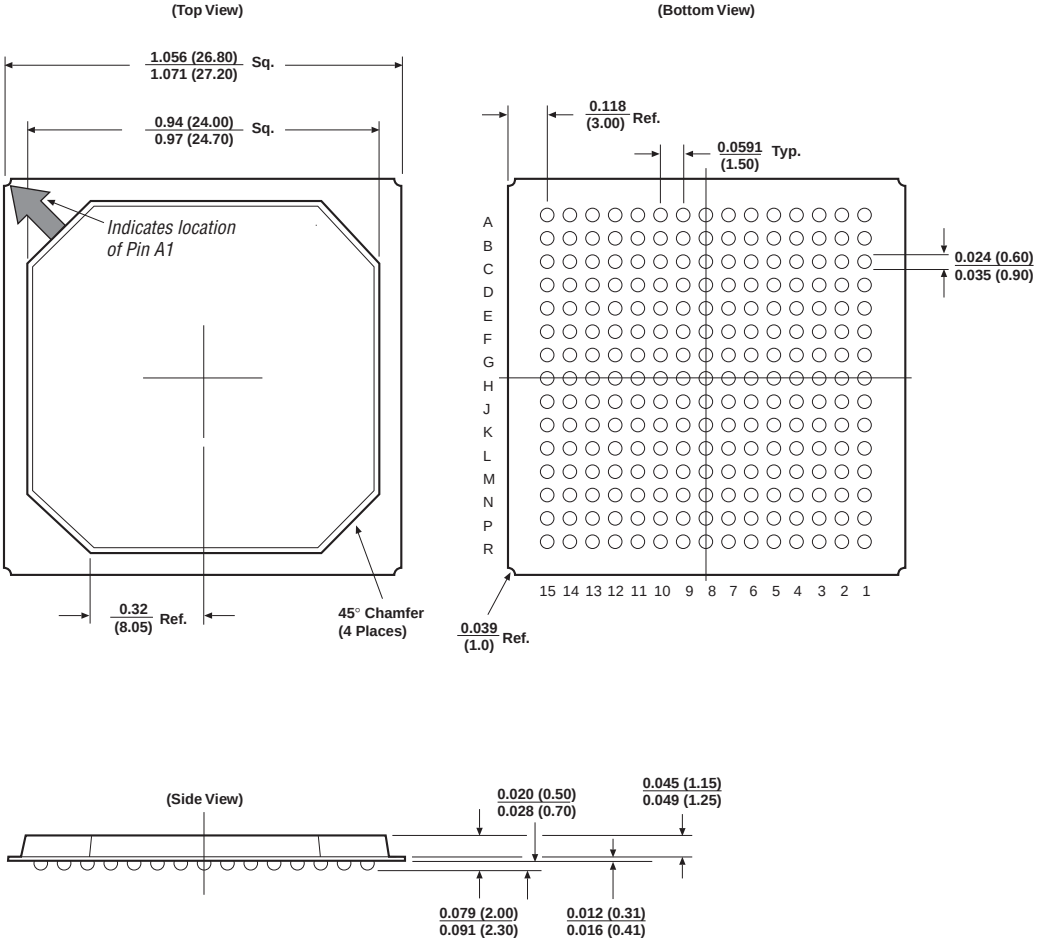
208-Pin Power Quad Flat Pack (RQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats. Metal heat sink is shown in the side view.



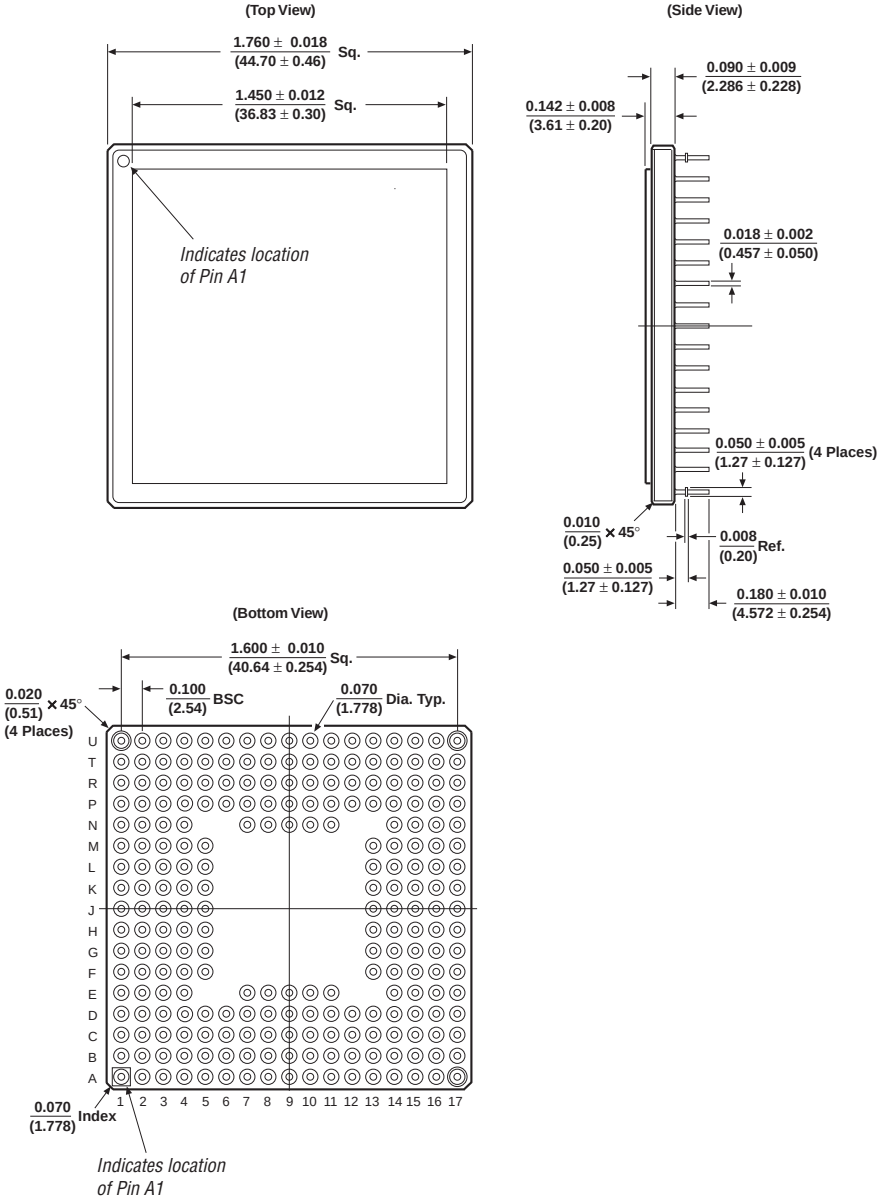
225-Pin Ball-Grid Array (BGA)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



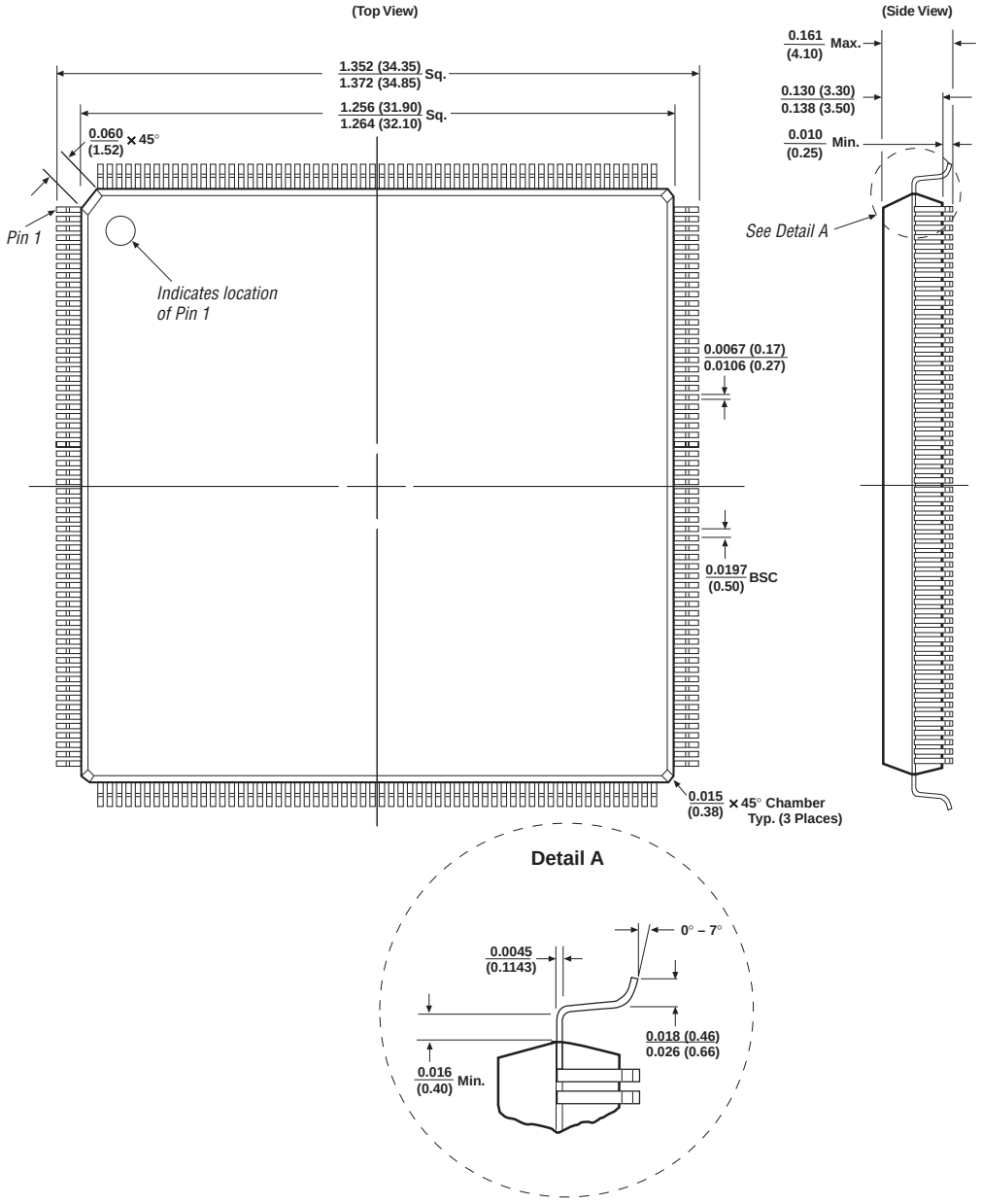
232-Pin Ceramic Pin-Grid Array (PGA)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



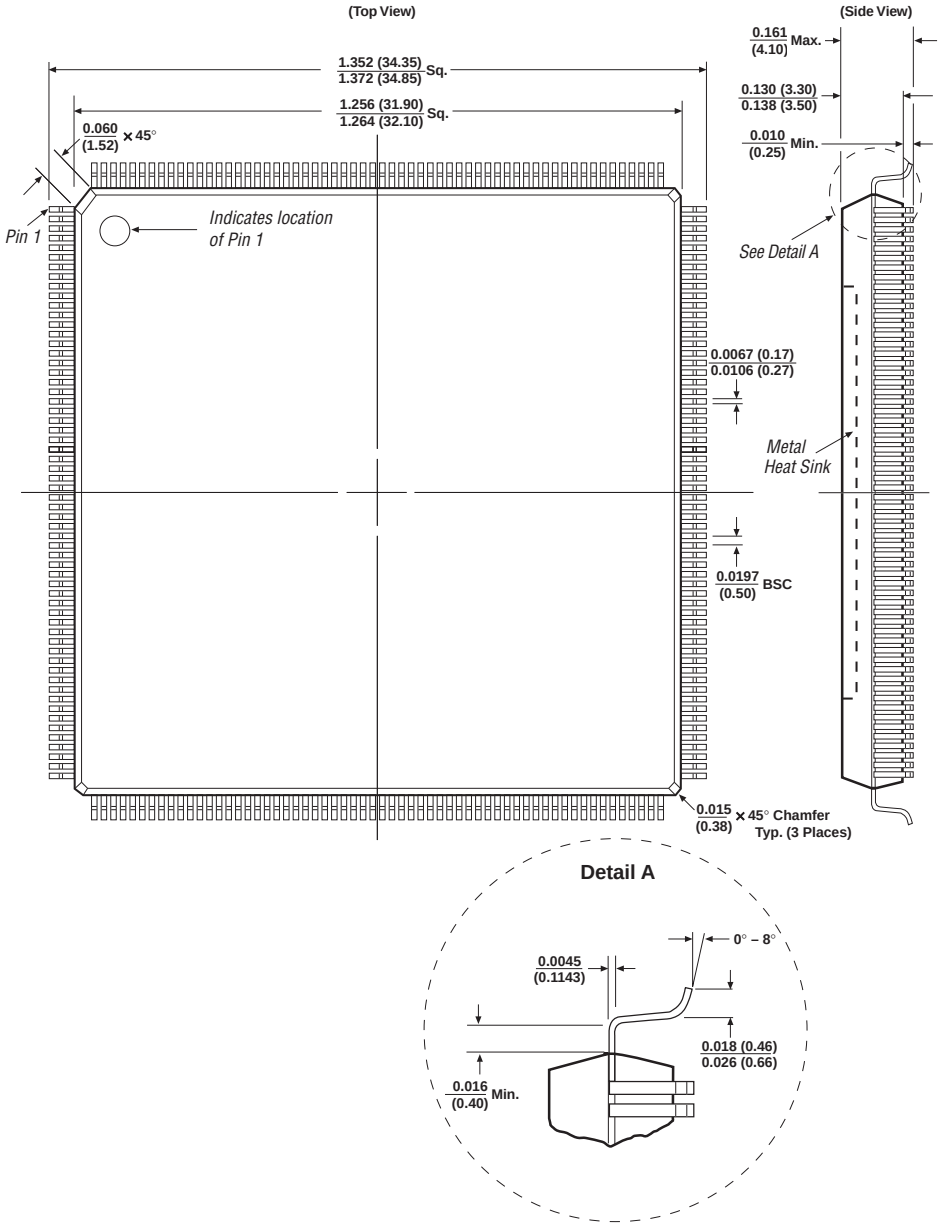
240-Pin Plastic Quad Flat Pack (PQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



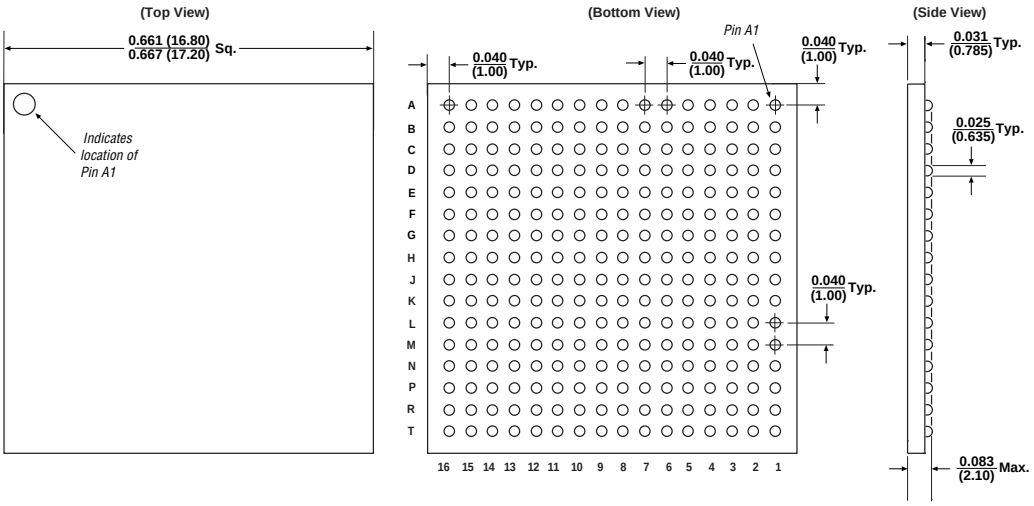
240-Pin Power Quad Flat Pack (RQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats. Metal heat sink is shown in the side view.



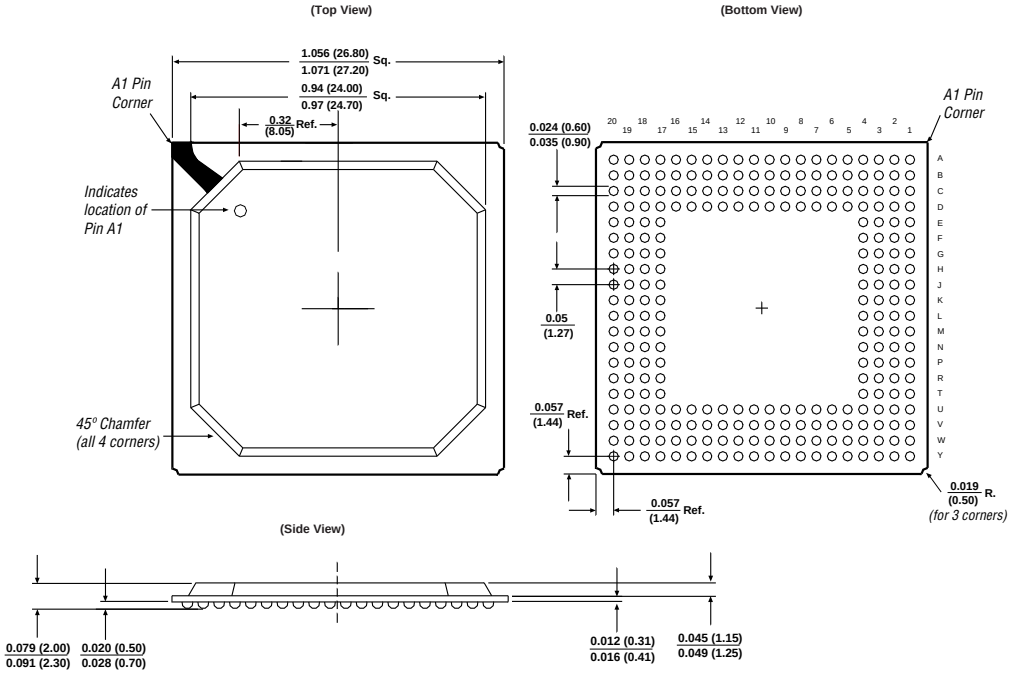
256-Pin FineLine BGA

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



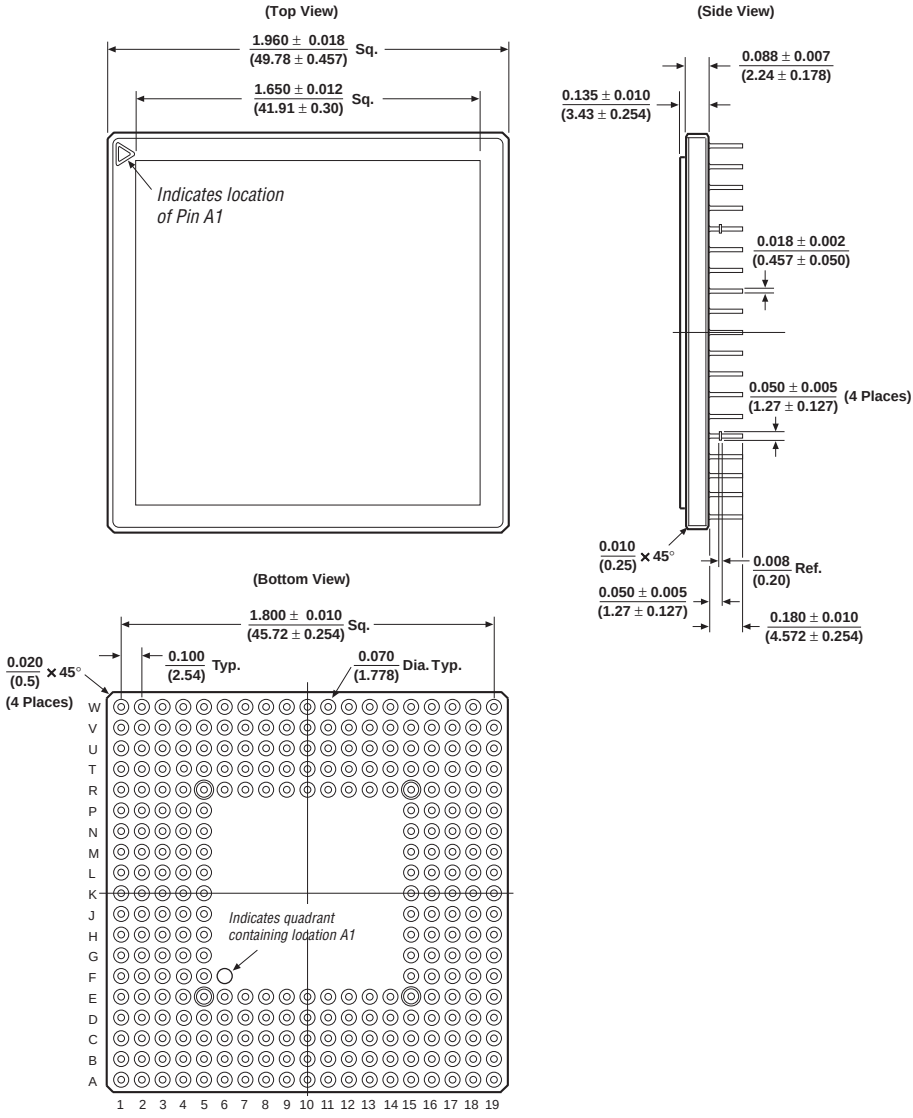
256-Pin Ball-Grid Array (BGA)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats. Metal heat sink is shown in the side view.



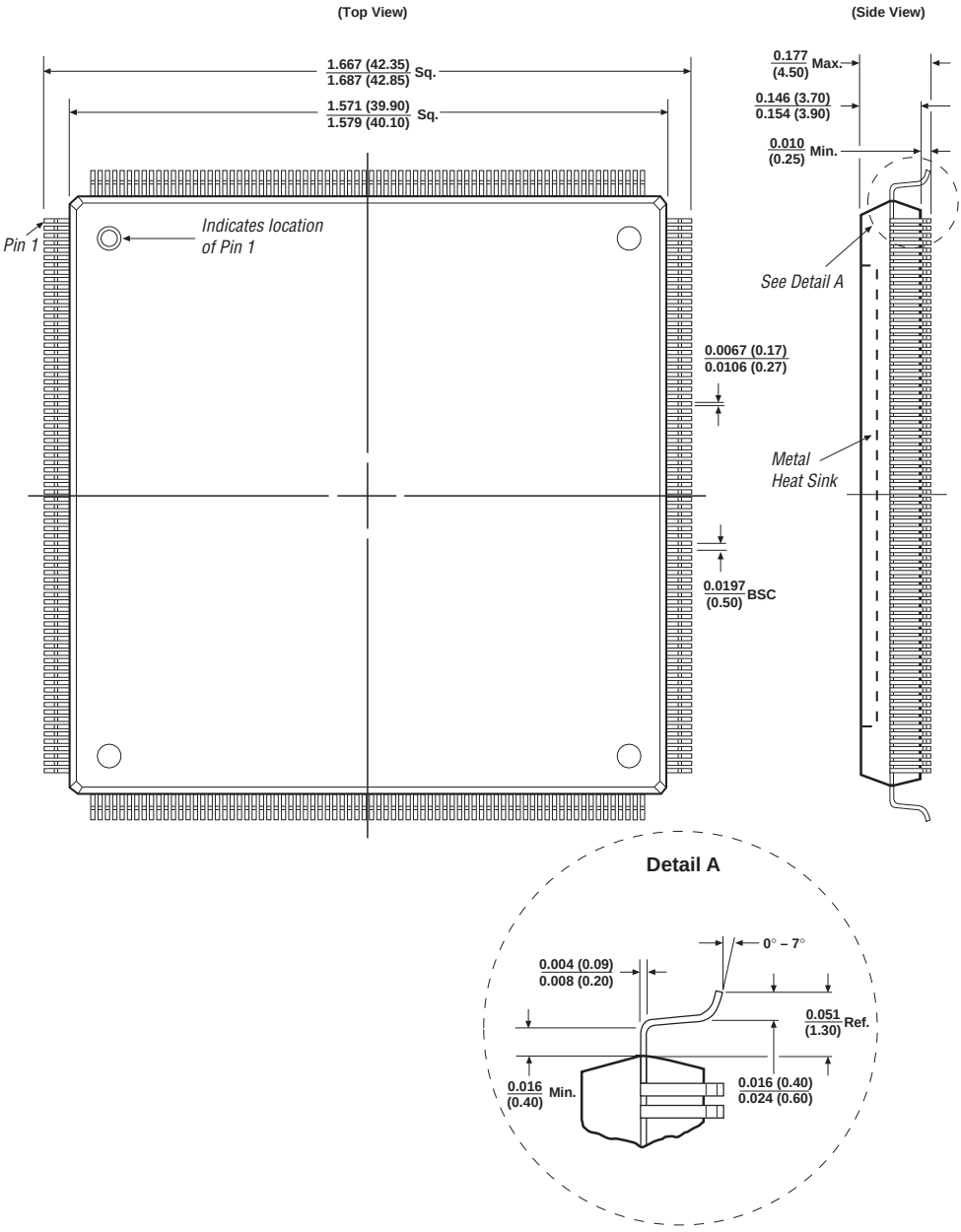
280-Pin Pin-Grid Array (PGA)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



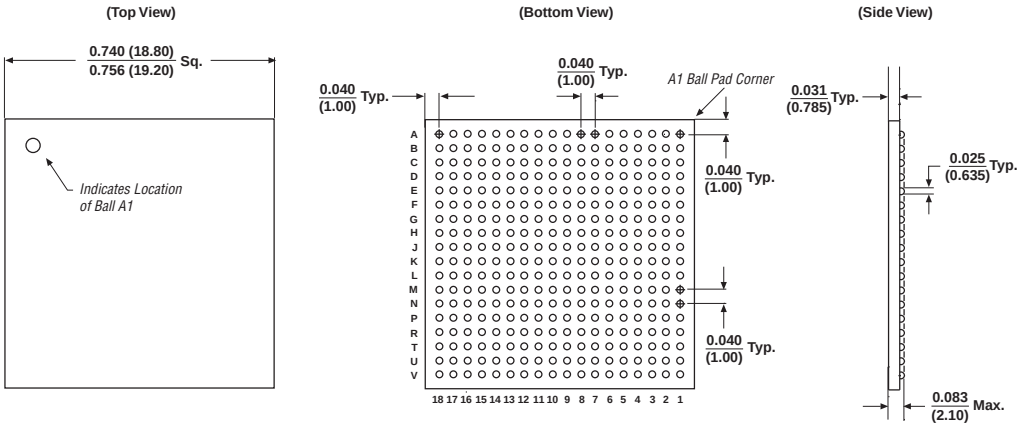
304-Pin Power Quad Flat Pack (RQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats. Metal heat sink is shown in the side view.



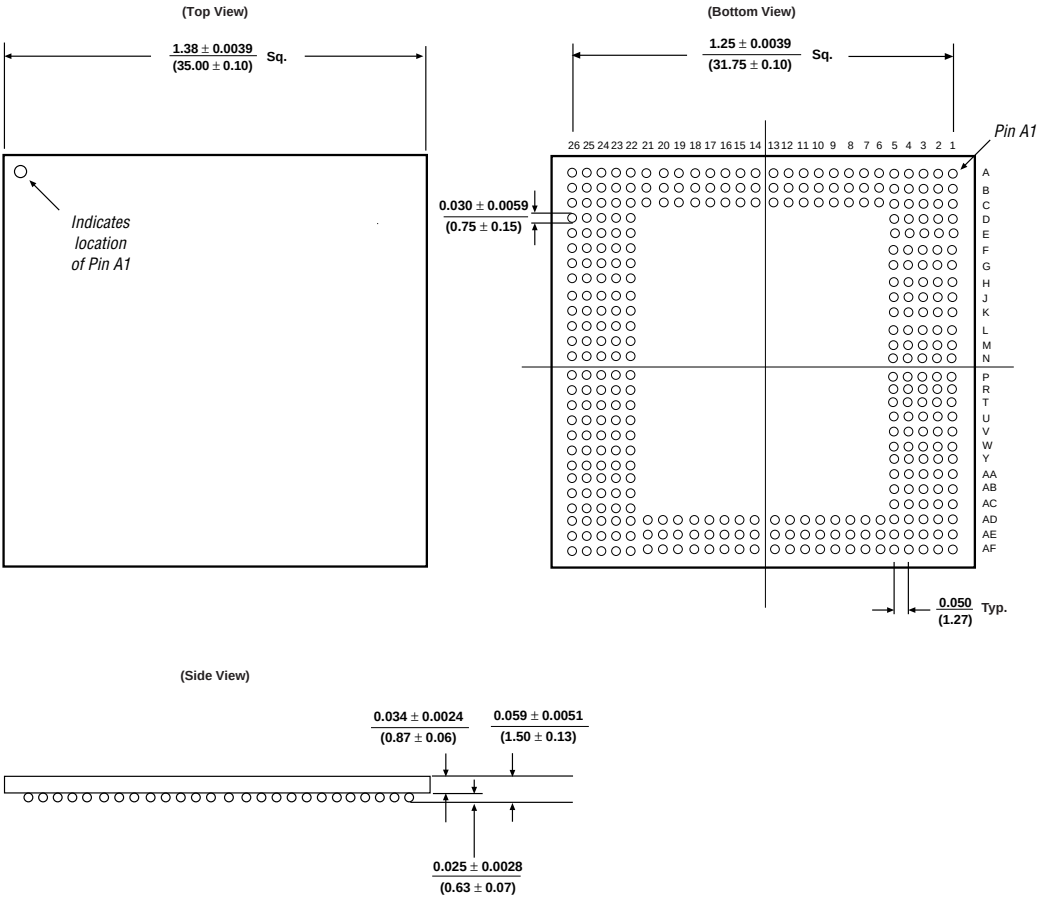
324-Pin FineLine BGA

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats. Metal heat sink is shown in the side view.



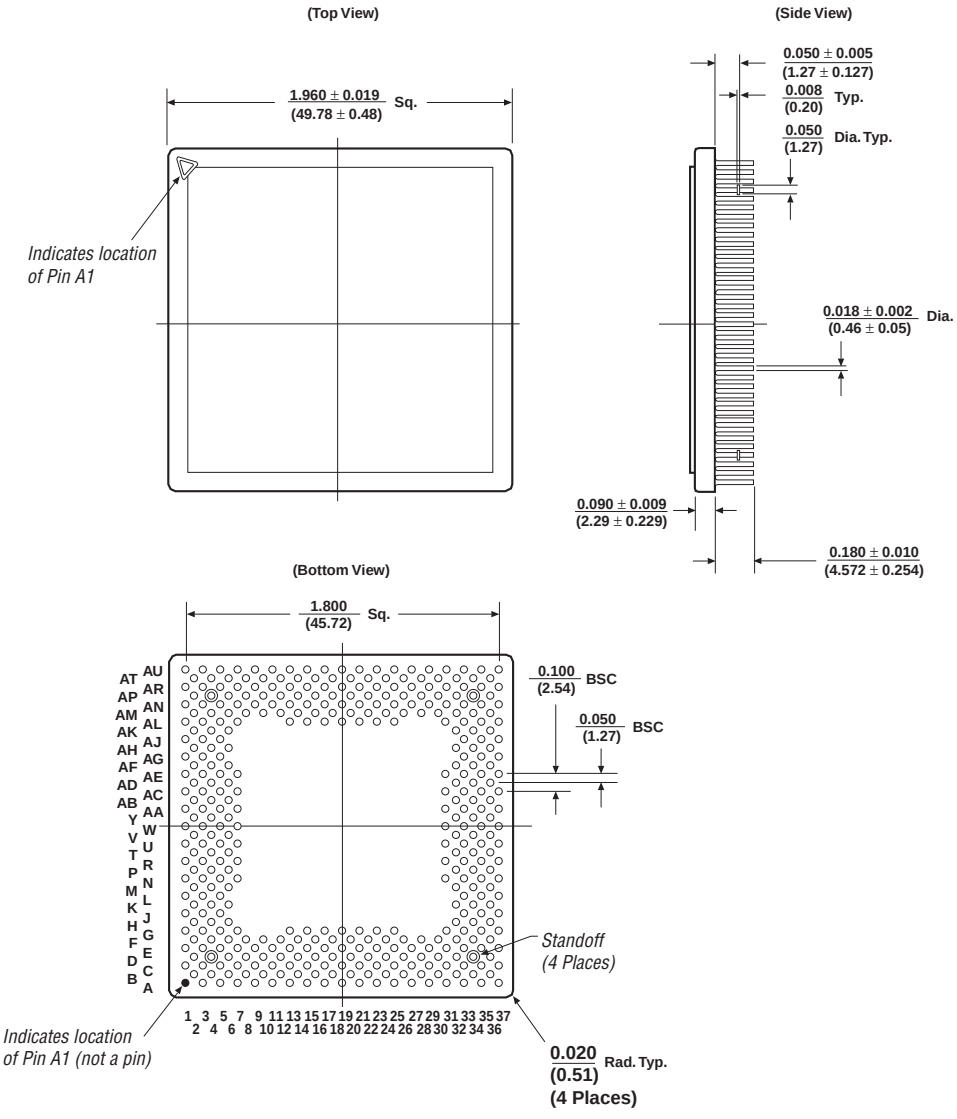
356-Pin Ball-Grid Array (BGA)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



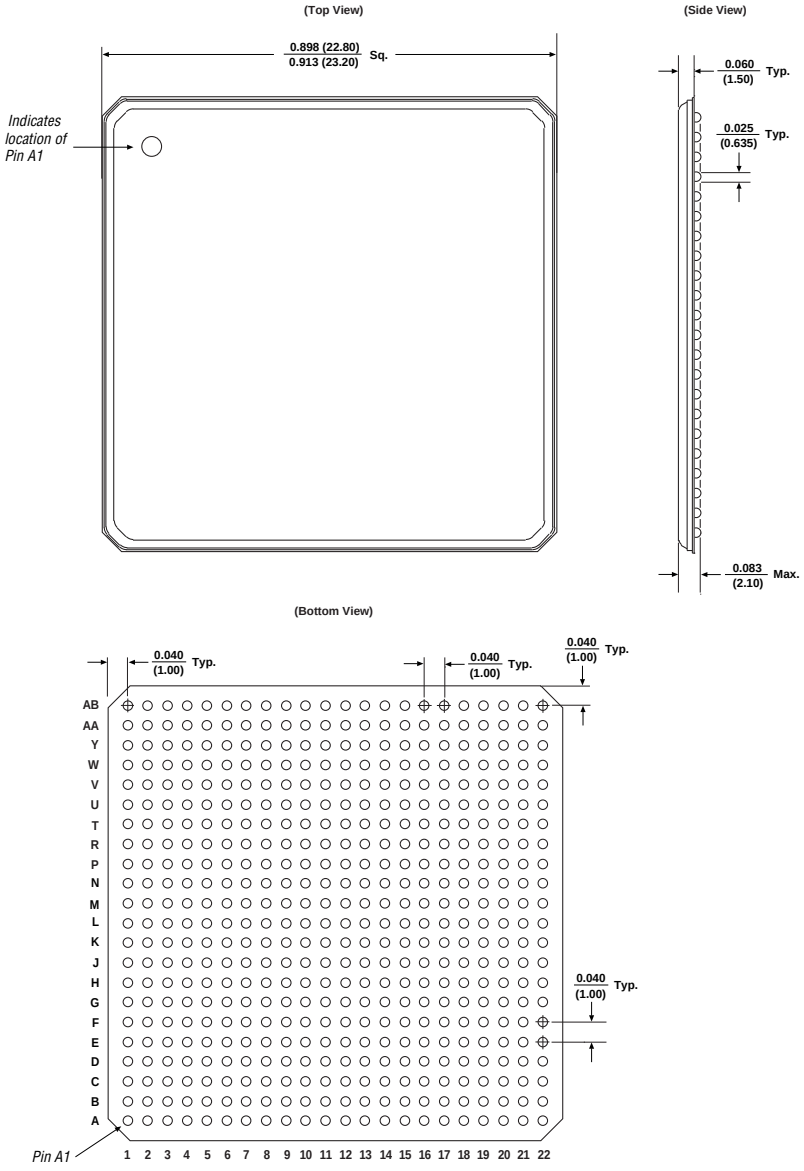
403-Pin Pin-Grid Array (PGA)

Controlling measurement is in inches. Millimeter measurements, shown in parenthesis, are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



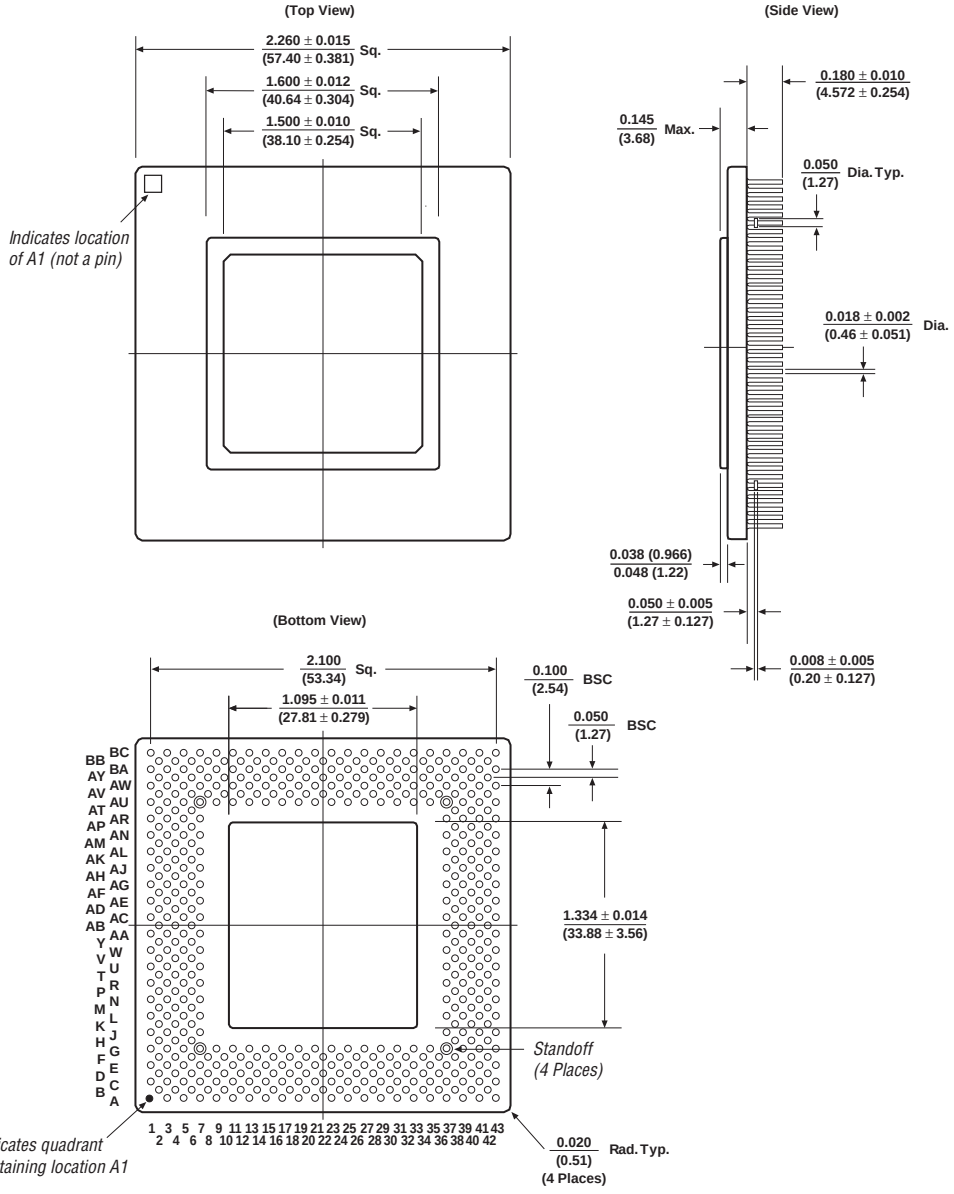
484-Pin FineLine BGA

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



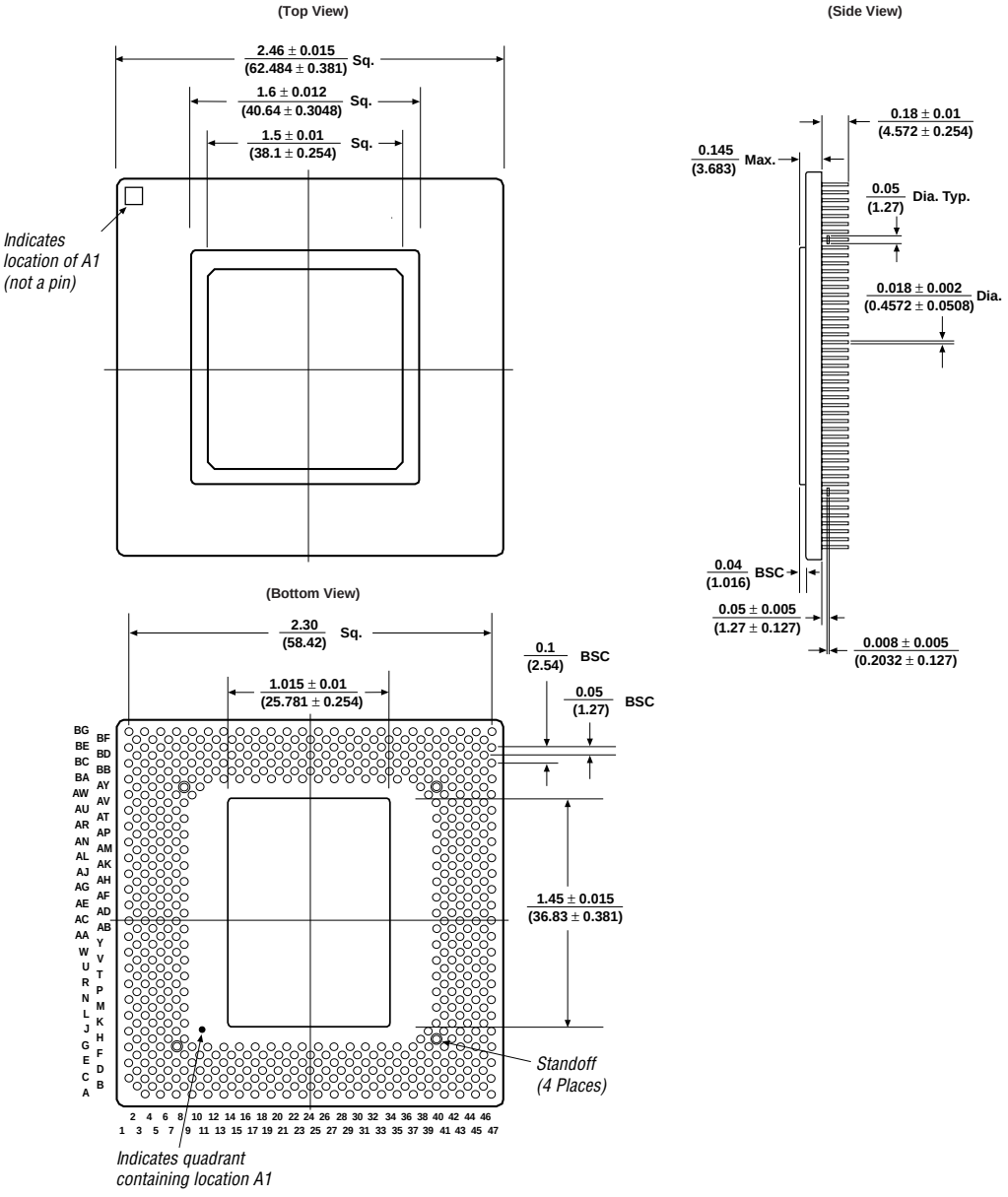
503-Pin Pin-Grid Array (PGA)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



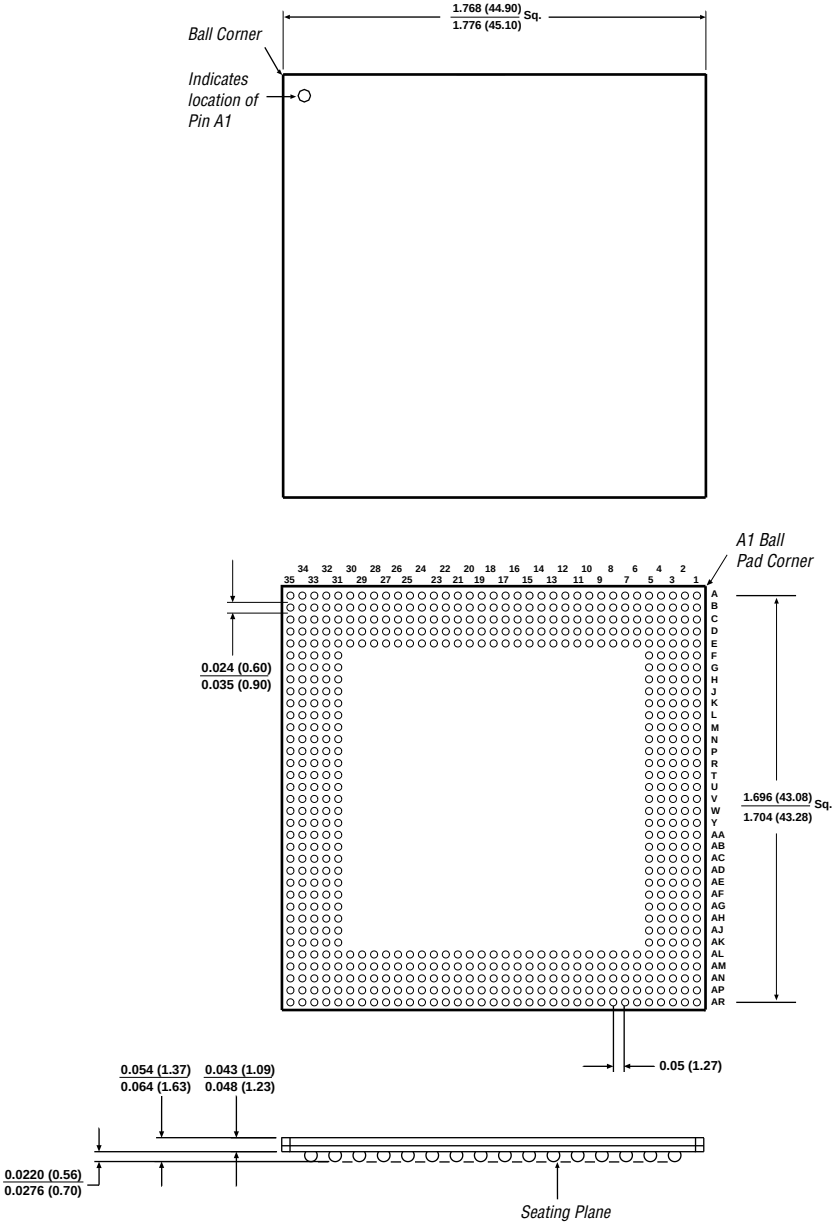
599-Pin Pin-Grid Array (PGA)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats. Metal heat sink is shown in the side view.



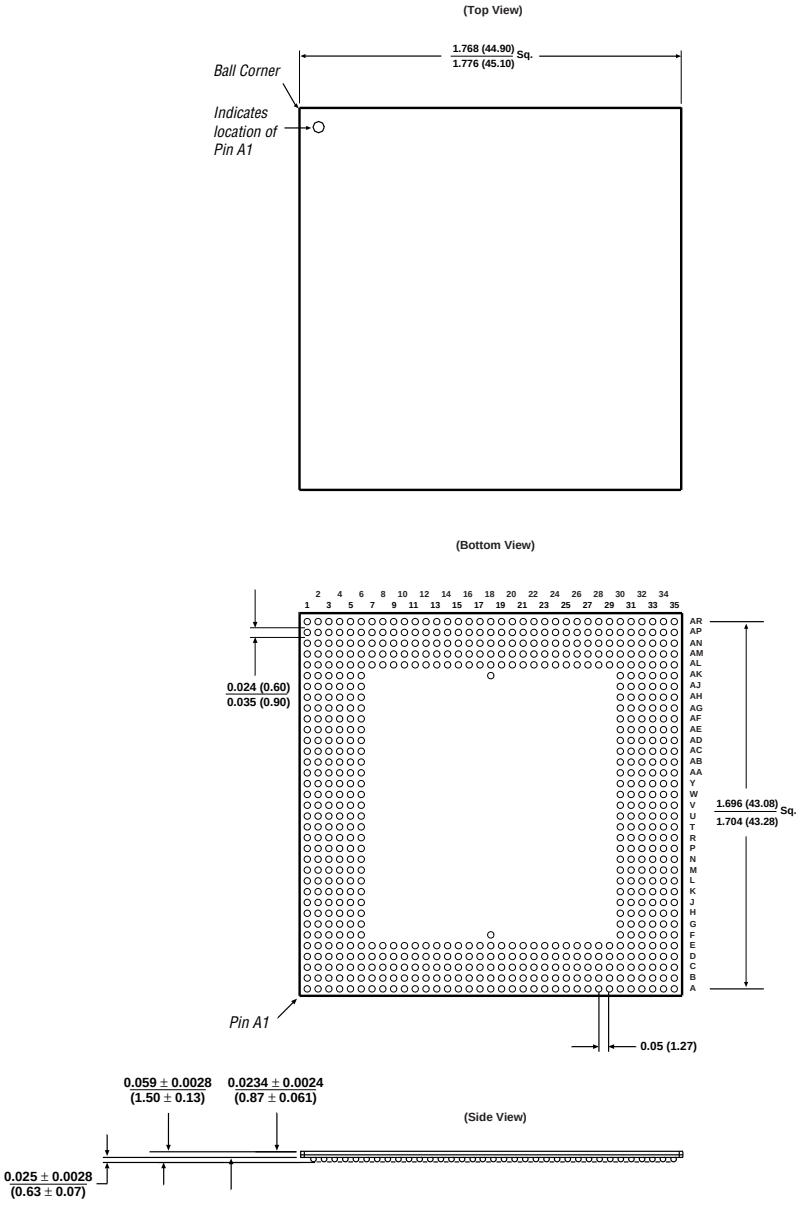
600-Pin Ball-Grid Array (BGA)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats. Metal heat sink is shown in the side view.



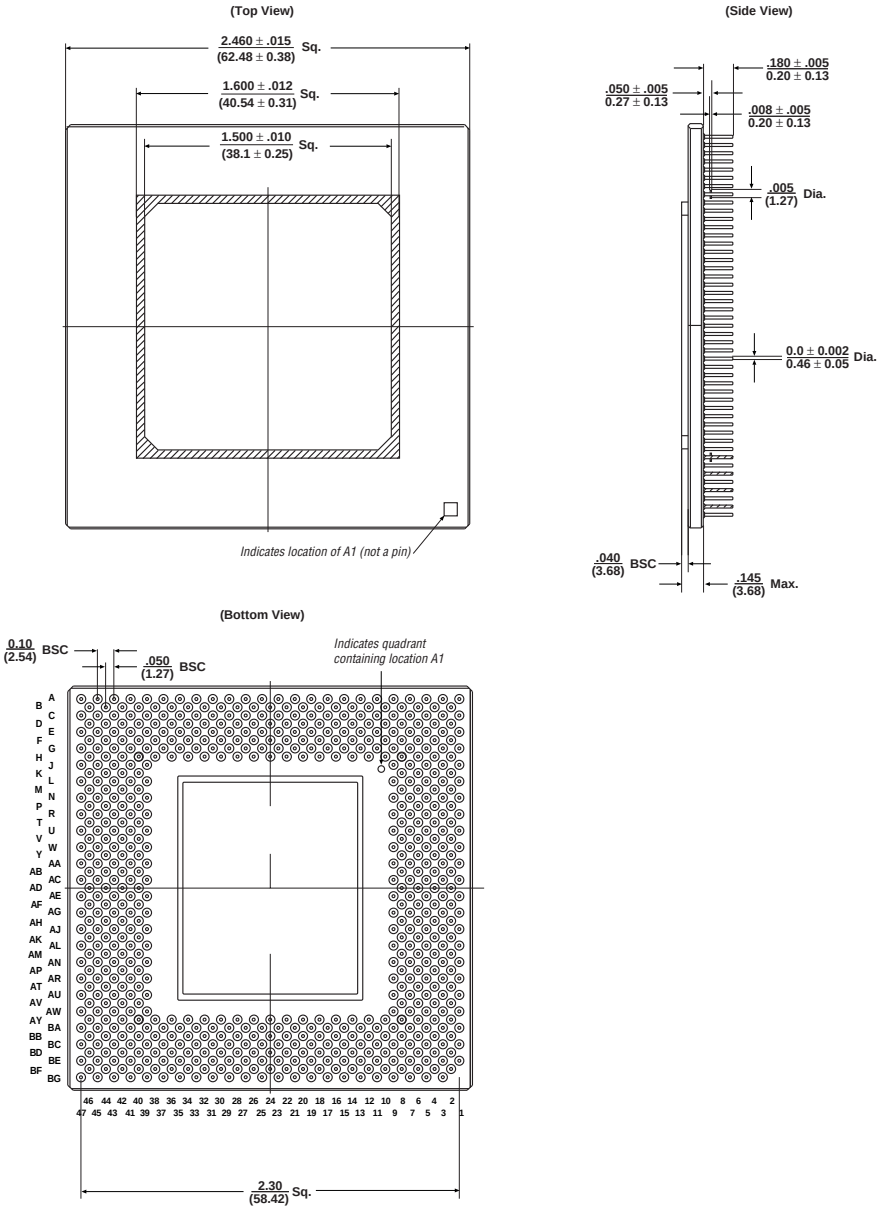
652-Pin Ball-Grid Array (BGA)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



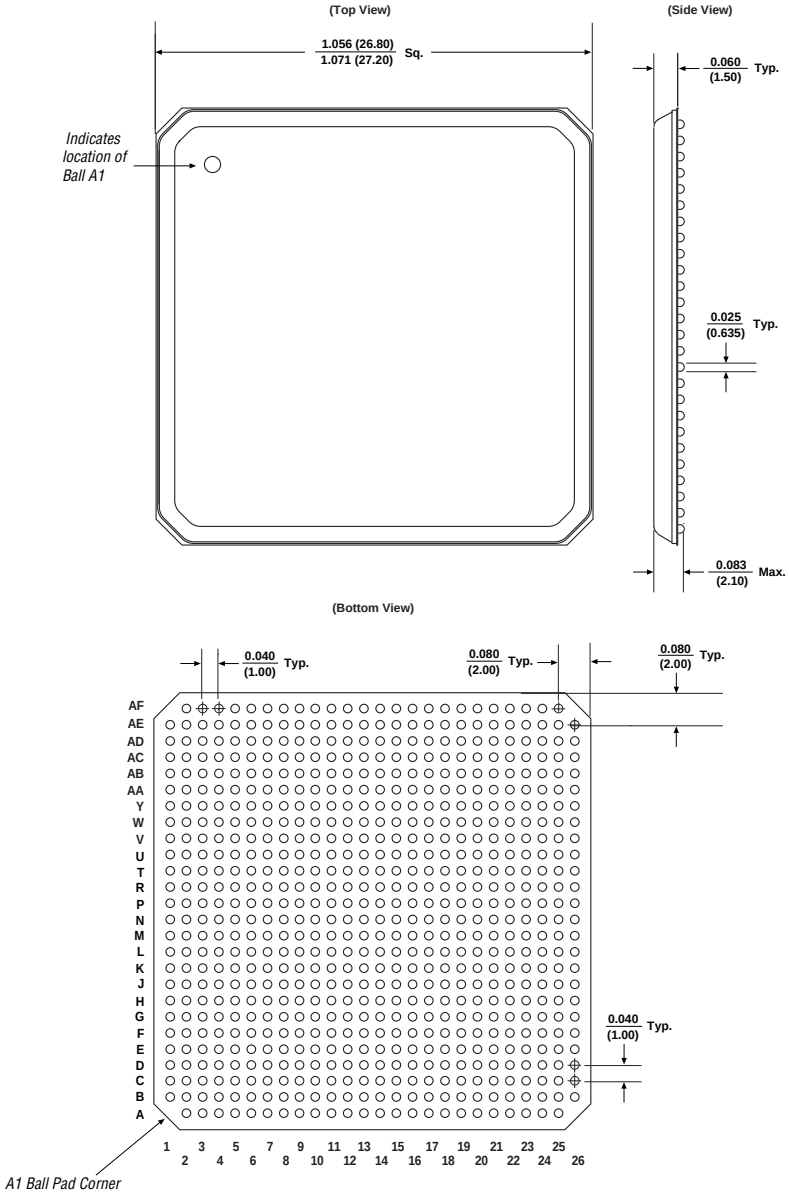
655-Pin Pin-Grid Array (PGA)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



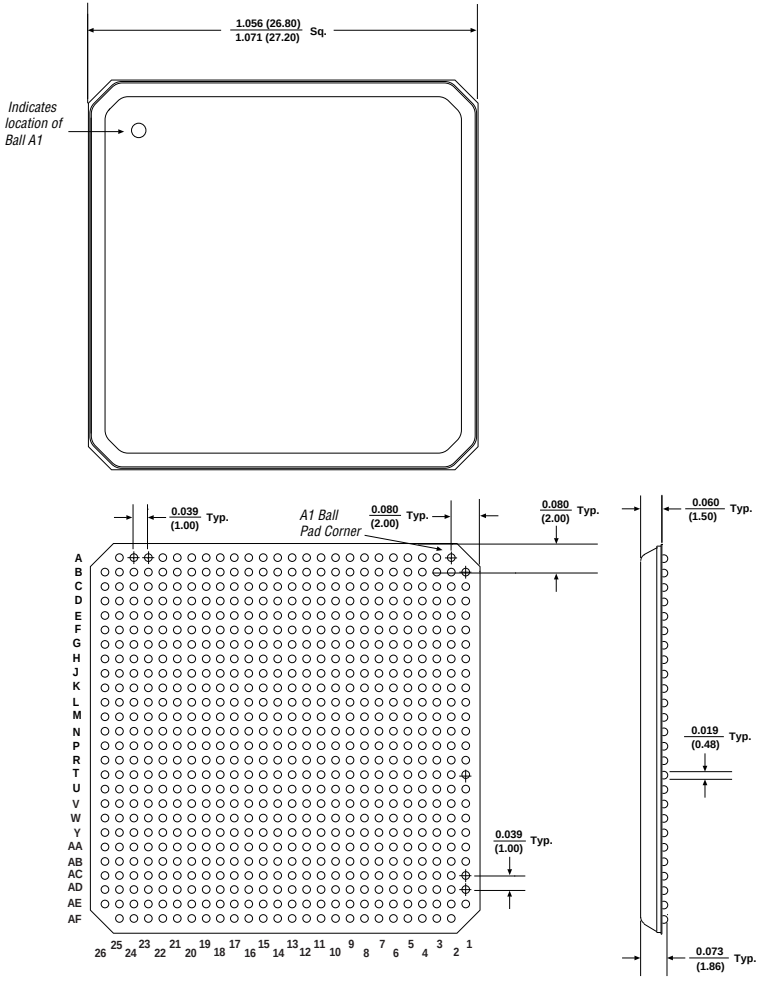
672-Pin FineLine BGA

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



672-Pin Thermally Enhanced FineLine BGA *Note (1)*

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Dimension Formats" on page 2-22 of this data sheet for dimension formats.



Note:
(1) Only available in APEX 20K devices.

Revision History

The information contained in the Device Package Information Data Sheet version 8.03 supersedes information published in previous versions.

Version 8.03 contains the following changes:

- Included thermal resistance values for the flip chip device package in Table 2 on page 2.
- Updated A1 ball pad corner placement on page 2-62.
- Adjusted arrow placement on page 2-68.
- Updated figure on page 2-68 with the proper side view values.
- Added 49-pin Ultra FineLine figure on page 2-36.
- Added 169-pin Ultra FineLine figure on page 2-49.
- Included Ultra FineLine BGA information in Table 1 on page 1.
- Updated Table 7 on page 9 with Ultra FineLine BGA information.
- Updated Tables 12, 13 and 14 page 2-16 with Ultra FineLine BGA information.

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
1	1	I/O	–	C6	C5
1	2	I/O	–	B5	D5
–	3	VCCINT	VCCINT	VCCINT	VCCINT
–	4	GNDINT	GND	GND	GND
1	5	I/O	–	A5	E4
1	6	I/O	–	B4	E5
1	7	I/O	–	A4	E6
–	8	VCCIO	VCCIO1	VCCIO1	VCCIO1
–	9	VCCIO	VCCIO8	VCCIO8	VCCIO8
8	10	I/O	–	–	F5
8	11	I/O	F6	E5	F6
8	12	I/O	–	–	G5
8	13	I/O	F5	E3	G6
–	14	VCCINT	VCCINT	VCCINT	VCCINT
–	15	GNDINT	GND	GND	GND
8	16	I/O	–	–	G7
8	17	I/O	–	–	H4
8	18	I/O	F4	F5	H5
8	19	I/O	–	–	H6
8	20	I/O	C1	F4	H7
–	21	GNDIO	GND	GND	GND
8	22	I/O	–	–	J4
8	23	I/O	–	–	J5
8	24	I/O	D1	E4	J6
8	25	I/O	–	–	J7
8	26	I/O	E2	F3	J8
–	27	VCCINT	VCCINT	VCCINT	VCCINT
–	28	GNDINT	GND	GND	GND
8	29	I/O	–	–	K4
8	30	I/O	–	–	K5
8	31	I/O	G6	D5	K6
8	32	I/O	–	–	K7
8	33	I/O	G5	G5	K8
–	34	VCCIO	VCCIO8	VCCIO8	VCCIO8
8	35	I/O	–	–	L5
8	36	I/O	–	–	L6
8	37	I/O	G4	G3	L7
8	38	I/O	–	–	L8
8	39	I/O	G3	G8	M5
–	40	VCCINT	VCCINT	VCCINT	VCCINT
–	41	GNDINT	GND	GND	GND
8	42	I/O	–	–	M6
8	43	I/O	–	–	M7
8	44	I/O	F2	G4	M8
8	45	I/O	–	–	M9
8	46	I/O	E1	C4	M10
–	47	GNDIO	GND	GND	GND
8	48	I/O	–	–	M11

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
8	49	I/O	–	–	N4
8	50	I/O	G2	G6	N5
8	51	I/O	–	–	N6
8	52	I/O	H6	H5	N7
–	53	VCCINT	VCCINT	VCCINT	VCCINT
–	54	GNDINT	GND	GND	GND
–	55	VCCINT	VCCINT	VCCINT	VCCINT
–	56	GNDINT	GND	GND	GND
8	57	I/O	H4	G7	N8
8	58	I/O	H3	H7	N9
8	59	I/O	F1	H4	N10
8	60	I/O	H2	H6	N11
8	61	I/O	G1	K7	P4
–	62	VCCIO	VCCIO8	VCCIO8	VCCIO8
8	63	I/O	J6	J5	P5
8	64	I/O	J5	H9	P6
8	65	I/O	J4	J8	P7
8	66	I/O	J3	H3	P8
8	67	I/O	J2	K3	P10
–	68	VCCINT	VCCINT	VCCINT	VCCINT
–	69	GNDINT	GND	GND	GND
8	70	I/O	J1	J4	P11
8	71	I/O	K6	K5	R4
8	72	I/O	K5	J6	R5
8	73	I/O	K4	L6	R6
8	74	I/O	K3	J7	R7
–	75	GNDIO	GND	GND	GND
8	76	I/O	K2	J3	R8
8	77	I/O	K1	K8	R10
8	78	I/O, DATA6 (1)	L6	L8	A4
8	79	I/O	L5	K6	R9
8	80	I/O	L4	K4	R11
–	81	VCCINT	VCCINT	VCCINT	VCCINT
–	82	GNDINT	GND	GND	GND
8	83	I/O	L2	N5	T4
8	84	I/O	L1	M8	T5
8	85	I/O, DATA7 (1)	M6	M10	B4
8	86	I/O	M5	M6	T6
8	87	I/O	M4	L7	T7
–	88	VCCIO	VCCIO8	VCCIO8	VCCIO8
8	89	I/O	M3	L9	T8
8	90	I/O	M2	M7	T10
8	91	I/O, nWS (1)	M1	P9	C4
8	92	I/O	N6	L5	T11
8	93	I/O	N5	P8	U4
–	94	VCCINT	VCCINT	VCCINT	VCCINT
–	95	GNDINT	GND	GND	GND
8	96	I/O	N3	L4	U5

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
8	97	I/O	N2	L3	U6
8	98	I/O, nRS (1)	N1	N10	D4
8	99	I/O	P6	R4	U7
8	100	I/O	P5	M5	U8
–	101	GNDIO	GND	GND	GND
8	102	I/O	P4	M3	U9
8	103	I/O	P3	P4	U10
8	104	I/O, nCS (1)	P2	M9	D3
8	105	I/O	P1	R3	U11
8	106	I/O	R6	P5	V4
–	107	VCCINT	VCCINT	VCCINT	VCCINT
–	108	GNDINT	GND	GND	GND
–	109	VCC_CKLK4 (2)	R4	P10	P9
–	110	GND_CKLK4 (2)	R3	R10	T9
–	111	GND_CKLK4 (2)	R3	R10	T9
8	112	I/O, CS (1)	R2	T6	E3
8	113	I/O	R1	M4	V5
8	114	I/O, DEV_CLRn (3)	T6	R9	H3
–	115	VCCIO	VCCIO8	VCCIO8	VCCIO8
8	116	I/O, CLKLK_FB2n (4)	T5	T8	J3
–	117	CLKLK_FB2p	T4	U8	K3
8	118	I/O, CLK4n (4)	T3	R7	N3
–	119	CLK4p	T2	R6	P3
8	120	I/O, CLK2n (4)	T1	N9	R3
–	121	VCCINT	VCCINT	VCCINT	VCCINT
–	122	GNDINT	GND	GND	GND
–	123	DATA0 (5), (6)	U4	N6	V3
–	124	DCLK (5)	U3	N7	W3
–	125	CLK2p	U2	N8	Y3
–	126	NCE (5)	U1	P6	AC3
–	127	TDI (5)	W1	P7	AD3
–	128	GND_CKLK2 (2)	W2	P11	V9
–	129	GND_CKLK2 (2)	W2	P11	V9
–	130	GNDINT	GND	GND	GND
–	131	VCCINT	VCCINT	VCCINT	VCCINT
–	132	VCC_CKLK2 (2)	W4	N11	Y9
7	133	I/O, DEV_OE (3)	Y5	R8	AE3
–	134	VCC_CKOUT2 (7)	Y1	V7	AA9
–	135	GND_CKOUT2 (7)	Y2	V6	W9
–	136	CLKLK_OUT2p (8)	Y3	T7	AH3
7	137	I/O, CLKLK_OUT2n (4)	Y4	U7	AJ3
–	138	GNDIO	GND	GND	GND
7	139	I/O, LVDSTXINCLK1p	W5	D1	AM5
7	140	I/O, LVDSTXINCLK1n (4)	Y6	D2	AL5
7	141	I/O, LOCK2 (9)	AB6	U6	AK4

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
7	142	I/O, LVDSTXOUTCLK1n (4)	AA2	E1	AM4
7	143	I/O, LVDSTXOUTCLK1p	AA3	E2	AL4
–	144	GNDINT	GND	GND	GND
–	145	VCCINT	VCCINT	VCCINT	VCCINT
7	146	I/O, LVDSTX01p	AA5	F1	D1
7	147	I/O, LVDSTX01n (4)	AA6	F2	D2
7	148	I/O	AA1	R5	V6
7	149	I/O, LVDSTX02n (4)	AB2	G1	E1
7	150	I/O, LVDSTX02p	AB3	G2	E2
–	151	VCCIO	VCCIO7	VCCIO7	VCCIO7
7	152	I/O, LVDSTX03p	AB4	H1	H1
7	153	I/O, LVDSTX03n (4)	AB5	H2	H2
7	154	I/O	AB1	T5	V7
7	155	I/O, LVDSTX04n (4)	AC1	J1	J1
7	156	I/O, LVDSTX04p	AC2	J2	J2
–	157	GNDINT	GND	GND	GND
–	158	VCCINT	VCCINT	VCCINT	VCCINT
7	159	I/O, LVDSTX05p	AC4	K1	K1
7	160	I/O, LVDSTX05n (4)	AC5	K2	K2
7	161	I/O, LOCK4 (9)	AC6	W7	AK5
7	162	I/O, LVDSTX06n (4)	AD1	L1	N1
7	163	I/O, LVDSTX06p	AD2	L2	N2
–	164	GNDIO	GND	GND	GND
7	165	I/O, LVDSTX07p	AD3	M1	P1
7	166	I/O, LVDSTX07n (4)	AD4	M2	P2
7	167	I/O	AD5	T3	V8
7	168	I/O, LVDSTX08n (4)	AD6	R1	R1
7	169	I/O, LVDSTX08p	AE1	R2	R2
–	170	GNDINT	GND	GND	GND
–	171	VCCINT	VCCINT	VCCINT	VCCINT
7	172	I/O, LVDSTX09p	AE3	T1	V1
7	173	I/O, LVDSTX09n (4)	AE4	T2	V2
7	174	I/O	AE5	U5	V10
7	175	I/O, LVDSTX10n (4)	AE6	U1	W1
7	176	I/O, LVDSTX10p	AF1	U2	W2
–	177	VCCIO	VCCIO7	VCCIO7	VCCIO7
7	178	I/O, LVDSTX11p	AF2	V1	Y1
7	179	I/O, LVDSTX11n (4)	AF3	V2	Y2
7	180	I/O	AF4	T4	V11
7	181	I/O, LVDSTX12n (4)	AF5	W1	AC1
7	182	I/O, LVDSTX12p	AF6	W2	AC2
–	183	GNDINT	GND	GND	GND
–	184	VCCINT	VCCINT	VCCINT	VCCINT
7	185	I/O, LVDSTX13p	AH1	Y1	AD1
7	186	I/O, LVDSTX13n (4)	AG2	Y2	AD2
7	187	I/O	AG3	U4	W4

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
7	188	I/O, LVDSTX14n (4)	AG4	AA1	AE1
7	189	I/O, LVDSTX14p	AG5	AA2	AE2
–	190	GNDIO	GND	GND	GND
7	191	I/O, LVDSTX15p	AG6	AB1	AH1
7	192	I/O, LVDSTX15n (4)	AJ1	AB2	AH2
7	193	I/O	AH2	W4	W5
7	194	I/O, LVDSTX16n (4)	AK1	AC1	AJ1
7	195	I/O, LVDSTX16p	AH3	AC2	AJ2
–	196	GNDINT	GND	GND	GND
–	197	VCCINT	VCCINT	VCCINT	VCCINT
–	198	GNDINT	GND	GND	GND
–	199	VCCINT	VCCINT	VCCINT	VCCINT
7	200	I/O	AH5	U3	W6
7	201	I/O	–	–	W7
7	202	I/O	AH6	V3	W8
7	203	I/O	–	–	W10
7	204	I/O	–	–	W11
–	205	VCCIO	VCCIO7	VCCIO7	VCCIO7
7	206	I/O	AJ2	W5	Y4
7	207	I/O	–	–	Y5
7	208	I/O	AL1	W6	Y6
7	209	I/O	–	–	Y7
7	210	I/O	–	–	Y8
–	211	GNDINT	GND	GND	GND
–	212	VCCINT	VCCINT	VCCINT	VCCINT
7	213	I/O	AK2	V5	Y10
7	214	I/O	–	–	Y11
7	215	I/O	AJ3	V4	AA5
7	216	I/O	–	–	AA6
7	217	I/O	–	–	AA7
–	218	GNDIO	GND	GND	GND
7	219	I/O	AJ4	W3	AA8
7	220	I/O	–	–	AA10
7	221	I/O	AJ5	Y5	AA11
7	222	I/O	–	–	AB5
7	223	I/O	–	–	AB6
–	224	GNDINT	GND	GND	GND
–	225	VCCINT	VCCINT	VCCINT	VCCINT
7	226	I/O	AJ6	AB5	AB7
7	227	I/O	–	–	AC4
7	228	I/O	AM1	AA5	AC5
7	229	I/O	–	–	AC6
7	230	I/O	–	–	AC7
–	231	VCCIO	VCCIO7	VCCIO7	VCCIO7
7	232	I/O	AK3	Y6	AD4
7	233	I/O	–	–	AD5
7	234	I/O	AK4	AA6	AD6
7	235	I/O	–	–	AD7

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
7	236	I/O	–	–	AE4
–	237	GNDINT	GND	GND	GND
–	238	VCCINT	VCCINT	VCCINT	VCCINT
7	239	I/O	AK5	AA7	AE5
7	240	I/O	–	–	AE6
7	241	I/O	AK6	AB6	AE7
7	242	I/O	–	–	AF5
–	243	GNDIO	GND	GND	GND
6	244	I/O	–	AB4	AF6
6	245	I/O	–	AA4	AG5
6	246	I/O	–	AC5	AG6
–	247	GNDINT	GND	GND	GND
–	248	VCCINT	VCCINT	VCCINT	VCCINT
6	249	I/O	–	Y4	AH4
6	250	I/O	–	AE4	AH5
6	251	I/O	AL7	AB3	AJ4
6	252	I/O	–	–	AJ5
6	253	I/O	AM6	AF4	AH6
6	254	I/O	–	–	AF7
6	255	I/O	AP3	Y3	AG7
–	256	VCCIO	VCCIO6	VCCIO6	VCCIO6
6	257	I/O	AN5	AD4	AH7
6	258	I/O	AR2	AA3	AB8
6	259	I/O	AP4	AE5	AC8
6	260	I/O	AL8	AD5	AD8
6	261	I/O	AM7	AD6	AE8
6	262	I/O	–	–	AF8
6	263	I/O	AN6	AB7	AG8
6	264	I/O	–	–	AH8
6	265	I/O	AR3	Y7	AJ8
6	266	I/O	–	–	AK8
–	267	GNDIO	GND	GND	GND
6	268	I/O	–	–	AL8
6	269	I/O	AP5	AC6	AM8
6	270	I/O	–	–	AB9
6	271	I/O	AL9	AB8	AC9
6	272	I/O	–	–	AD9
6	273	I/O	AR4	AF5	AE9
6	274	I/O	AM8	V8	AF9
6	275	I/O	AN7	AC7	AG9
6	276	I/O	AP6	AD7	AH9
6	277	I/O	AR5	T9	AJ9
–	278	VCCIO	VCCIO6	VCCIO6	VCCIO6
6	279	I/O	AM9	AE7	AK9
6	280	I/O	–	–	AL9
6	281	I/O	AL10	AA9	AM9
6	282	I/O	–	–	AB10
6	283	I/O	AN8	AF7	AC10

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
6	284	I/O	–	–	AD10
6	285	I/O	–	–	AE10
6	286	I/O	AP7	AA8	AF10
6	287	I/O	–	–	AG10
6	288	I/O	AR6	AC8	AH10
–	289	GNDIO	GND	GND	GND
6	290	I/O	–	–	AJ10
6	291	I/O	AM10	Y8	AK10
6	292	I/O	AN9	AD8	AL10
6	293	I/O	AL11	Y9	AB11
6	294	I/O	AP8	W9	AC11
6	295	I/O	AR7	AB9	AD11
6	296	I/O	AM11	W10	AE11
6	297	I/O	–	–	AF11
6	298	I/O	AN10	AC9	AG11
6	299	I/O	–	–	–
6	300	I/O	AP9	Y10	AH11
–	301	VCCIO	VCCIO6	VCCIO6	VCCIO6
–	302	VCCINT	VCCINT	VCCINT	VCCINT
–	303	VCCINT	VCCINT	VCCINT	VCCINT
–	304	GNDINT	GND	GND	GND
–	305	GNDINT	GND	GND	GND
6	306	I/O	AR8	AD9	AB12
6	307	I/O	–	–	–
6	308	I/O	AN11	AA10	AC12
6	309	I/O	–	–	AD12
6	310	I/O	AP10	AB11	AE12
6	311	I/O	AR9	V11	AF12
6	312	I/O	AL13	AB10	AG12
6	313	I/O	AM13	AC10	AH12
6	314	I/O	AN12	AA11	AB13
6	315	I/O	AP11	AE9	AC13
6	316	I/O	–	–	AD13
–	317	GNDIO	GND	GND	GND
6	318	I/O	AL14	Y11	AE13
6	319	I/O	–	–	AF13
6	320	I/O	AR10	AF9	AG13
6	321	I/O	–	–	AH13
6	322	I/O	–	–	AJ13
6	323	I/O	AN13	W11	AK13
6	324	I/O	–	–	AL13
6	325	I/O	AP12	AF11	AB14
6	326	I/O	–	–	AC14
6	327	I/O	AM14	V12	AD14
–	328	VCCIO	VCCIO6	VCCIO6	VCCIO6
6	329	I/O	AR11	AE10	AE14
6	330	I/O	AL15	W12	AF14
6	331	I/O	AN14	Y12	AG14

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
6	332	I/O	AP13	T13	AH14
6	333	I/O	AR12	W14	AJ14
6	334	I/O	–	–	AK14
6	335	I/O	AR13	AB12	AL14
6	336	I/O	–	–	AB15
6	337	I/O	AM15	AF10	AC15
6	338	I/O	–	–	AD15
–	339	GNDIO	GND	GND	GND
6	340	I/O	–	–	AE15
6	341	I/O	AN15	U13	AF15
6	342	I/O	–	–	AG15
6	343	I/O	AL16	W13	AH15
6	344	I/O	–	–	AJ15
6	345	I/O	AP14	AE11	AK15
6	346	I/O	AR14	V13	AL15
6	347	I/O	AP15	AD11	AB16
6	348	I/O	AR15	AD12	AC16
6	349	I/O, LVDSDESKEW	AM16	U12	AM10
–	350	VCCIO	VCCIO6	VCCIO6	VCCIO6
6	351	I/O	AN16	AE12	AD16
6	352	I/O	–	–	AE16
6	353	I/O	AP16	AF12	AF16
6	354	I/O	–	–	AG16
6	355	I/O	AR16	AE13	AH16
–	356	CONF_DONE (5)	AM17	AA12	AM13
–	357	NSTATUS (5)	AN17	AA13	AM14
5	358	FAST4	AP17	Y13	AM15
–	359	VCCINT	VCCINT	VCCINT	VCCINT
–	360	VCCINT	VCCINT	VCCINT	VCCINT
–	361	GNDINT	GND	GND	GND
–	362	GNDINT	GND	GND	GND
–	363	GNDIO	GND	GND	GND
5	364	FAST3	AP19	Y14	AM18
–	365	TCK (5)	AN19	AA14	AM19
–	366	TMS (5)	AM19	AA15	AM20
5	367	I/O	AR20	AE14	AJ16
5	368	I/O	–	–	AK16
5	369	I/O	AP20	AD14	AK17
5	370	I/O	–	–	AJ17
5	371	I/O	AN20	AE15	AH17
–	372	VCCIO	VCCIO5	VCCIO5	VCCIO5
5	373	I/O	AM20	AD15	AG17
5	374	I/O	AR21	AD16	AF17
5	375	I/O	AP21	AC13	AE17
5	376	I/O	AR22	AD17	AD17
5	377	I/O	AP22	AC12	AC17
5	378	I/O	–	–	AB17
5	379	I/O	AL20	AC14	AL18

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
5	380	I/O	–	–	AK18
5	381	I/O	AN21	AD10	AJ18
5	382	I/O	–	–	AH18
–	383	GNDIO	GND	GND	GND
5	384	I/O	–	–	AG18
5	385	I/O	AM21	AB13	AF18
5	386	I/O	–	–	AE18
5	387	I/O	AR23	V14	AD18
5	388	I/O	–	–	AC18
5	389	I/O	AR24	AB14	AB18
5	390	I/O	AP23	Y15	AL19
5	391	I/O	AN22	AC11	AK19
5	392	I/O	AL21	AD18	AJ19
5	393	I/O	AR25	U14	AH19
–	394	VCCIO	VCCIO5	VCCIO5	VCCIO5
5	395	I/O	AM22	AC15	AG19
5	396	I/O	–	–	AF19
5	397	I/O	AP24	V15	AE19
5	398	I/O	–	–	AD19
5	399	I/O	AN23	AB15	AC19
5	400	I/O	–	–	AB19
5	401	I/O	–	–	AL20
5	402	I/O	AR26	W15	AK20
5	403	I/O	–	–	AJ20
5	404	I/O	AL22	AB16	AH20
–	405	GNDIO	GND	GND	GND
5	406	I/O	–	–	AG20
5	407	I/O	AP25	T14	AF20
5	408	I/O	AN24	AD19	AE20
5	409	I/O	AM23	AA16	AD20
5	410	I/O	AL23	Y16	AC20
5	411	I/O	AR27	AC16	AB20
5	412	I/O	AP26	W16	AH21
5	413	I/O	–	–	AG21
5	414	I/O	AN25	AC17	AF21
5	415	I/O	–	–	–
5	416	I/O	AR28	U15	AE21
–	417	VCCIO	VCCIO5	VCCIO5	VCCIO5
–	418	VCCINT	VCCINT	VCCINT	VCCINT
–	419	VCCINT	VCCINT	VCCINT	VCCINT
–	420	GNDINT	GND	GND	GND
–	421	GNDINT	GND	GND	GND
5	422	I/O	AP27	AB17	AD21
5	423	I/O	–	–	–
5	424	I/O	AN26	V16	AC21
5	425	I/O	–	–	AB21
5	426	I/O	AM25	AE16	AH22
5	427	I/O	AR29	AA17	AG22

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
5	428	I/O	AP28	AD20	AF22
5	429	I/O	AL25	AB18	AE22
5	430	I/O	AN27	Y17	AD22
5	431	I/O	AM26	AF16	AC22
5	432	I/O	–	–	AB22
–	433	GNDIO	GND	GND	GND
5	434	I/O	AR30	AA18	AM23
5	435	I/O	–	–	AL23
5	436	I/O	AP29	AC18	AK23
5	437	I/O	–	–	AJ23
5	438	I/O	–	–	AH23
5	439	I/O	AN28	W17	AG23
5	440	I/O	–	–	AF23
5	441	I/O	AL26	AE17	AE23
5	442	I/O	–	–	AD23
5	443	I/O	AM27	Y18	AC23
–	444	VCCIO	VCCIO5	VCCIO5	VCCIO5
5	445	I/O	AR31	AF17	AB23
5	446	I/O	AP30	W18	AM24
5	447	I/O	AN29	AA19	AL24
5	448	I/O	AM28	AD21	AK24
5	449	I/O	AR32	Y19	AJ24
5	450	I/O	–	–	AH24
5	451	I/O	AL27	AD22	AG24
5	452	I/O	–	–	AF24
5	453	I/O	AP31	W20	AE24
5	454	I/O	–	–	AD24
–	455	GNDIO	GND	GND	GND
5	456	I/O	–	–	AC24
5	457	I/O	AR33	AC19	AB24
5	458	I/O	–	–	AM25
5	459	I/O	AN30	Y20	AL25
5	460	I/O	–	–	AK25
5	461	I/O	AM29	AB20	AJ25
5	462	I/O	AL28	AB19	AH25
5	463	I/O	AP32	AC20	AG25
5	464	I/O	AR34	AD23	AF25
5	465	I/O	AN31	AA20	AE25
–	466	VCCIO	VCCIO5	VCCIO5	VCCIO5
5	467	I/O	AP33	AB24	AD25
5	468	I/O	–	–	AC25
5	469	I/O	AM30	AC22	AB25
5	470	I/O	–	–	AH26
5	471	I/O	AL29	AC21	AG26
5	472	I/O	–	Y23	AF26
5	473	I/O	–	Y24	AH27
–	474	VCCINT	VCCINT	VCCINT	VCCINT
–	475	GNDINT	GND	GND	GND

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
5	476	I/O	–	AA23	AK28
5	477	I/O	–	AA24	AK29
5	478	I/O	–	AB23	AJ28
–	479	GNDIO	GND	GND	GND
4	480	I/O	–	–	AJ29
4	481	I/O	AL33	AA21	AJ30
4	482	I/O	–	–	AH28
4	483	I/O	AK30	Y22	AH29
–	484	VCCINT	VCCINT	VCCINT	VCCINT
–	485	GNDINT	GND	GND	GND
4	486	I/O	–	–	AH30
4	487	I/O	–	–	AG27
4	488	I/O	AK31	AB21	AG28
4	489	I/O	–	–	AF27
4	490	I/O	AK32	U19	AF28
–	491	VCCIO	VCCIO4	VCCIO4	VCCIO4
4	492	I/O	–	–	AE26
4	493	I/O	–	–	AE27
4	494	I/O	AL34	AB22	AE28
4	495	I/O	–	–	AE29
4	496	I/O	AM35	V19	AE30
–	497	VCCINT	VCCINT	VCCINT	VCCINT
–	498	GNDINT	GND	GND	GND
4	499	I/O	–	–	AD26
4	500	I/O	–	–	AD27
4	501	I/O	AJ30	T18	AD28
4	502	I/O	–	–	AD29
4	503	I/O	AJ31	W21	AD30
–	504	GNDIO	GND	GND	GND
4	505	I/O	–	–	AC26
4	506	I/O	–	–	AC27
4	507	I/O	AJ32	V20	AC28
4	508	I/O	–	–	AC29
4	509	I/O	AJ33	V21	AB26
–	510	VCCINT	VCCINT	VCCINT	VCCINT
–	511	GNDINT	GND	GND	GND
4	512	I/O	–	–	AB27
4	513	I/O	–	–	AB28
4	514	I/O	AK34	Y21	AA22
4	515	I/O	–	–	AA23
4	516	I/O	AL35	W22	AA24
–	517	VCCIO	VCCIO4	VCCIO4	VCCIO4
4	518	I/O	–	–	AA25
4	519	I/O	–	–	AA26
4	520	I/O	AJ34	AA22	AA27
4	521	I/O	–	–	AA28
4	522	I/O	AH30	U20	Y22
–	523	VCCINT	VCCINT	VCCINT	VCCINT

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
–	524	GNDINT	GND	GND	GND
–	525	VCCINT	VCCINT	VCCINT	VCCINT
–	526	GNDINT	GND	GND	GND
4	527	I/O	AH32	R17	Y23
4	528	I/O	AH33	W23	Y24
4	529	I/O	AK35	T19	Y25
4	530	I/O	AH34	U21	Y26
4	531	I/O	AJ35	P17	Y27
–	532	GNDIO	GND	GND	GND
4	533	I/O	AG30	R18	Y28
4	534	I/O	AG31	W24	Y29
4	535	I/O	AG32	T20	W22
4	536	I/O	AG33	V24	W23
4	537	I/O	AG34	N16	W25
–	538	VCCINT	VCCINT	VCCINT	VCCINT
–	539	GNDINT	GND	GND	GND
4	540	I/O	AG35	V22	W26
4	541	I/O	AF30	R19	W27
4	542	I/O	AF31	V23	W28
4	543	I/O	AF32	P18	W29
4	544	I/O	AF33	N17	V22
–	545	VCCIO	VCCIO4	VCCIO4	VCCIO4
4	546	I/O	AF34	T21	V23
4	547	I/O	AF35	R21	V25
4	548	I/O	AE30	U22	V26
4	549	I/O	AE31	R20	V27
4	550	I/O	AE32	P22	V28
–	551	VCCINT	VCCINT	VCCINT	VCCINT
–	552	GNDINT	GND	GND	GND
4	553	I/O	AE34	N18	V29
4	554	I/O	AE35	U23	U22
4	555	I/O	AD30	N19	U23
4	556	I/O	AD31	N22	U24
4	557	I/O	AD32	L20	U25
–	558	GNDIO	GND	GND	GND
4	559	I/O	AD33	M17	U26
4	560	I/O	AD34	T22	U27
4	561	I/O	AD35	M18	U28
4	562	I/O	AC30	T23	U29
4	563	I/O	AC31	R23	T22
–	564	VCCINT	VCCINT	VCCINT	VCCINT
–	565	GNDINT	GND	GND	GND
4	566	I/O	AC33	U24	T23
4	567	I/O	AC34	R24	T25
4	568	I/O	AC35	T24	T26
4	569	I/O	AB30	M21	T27
4	570	I/O	AB31	M24	T28
–	571	VCCIO	VCCIO4	VCCIO4	VCCIO4

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
4	572	I/O	AB32	M22	T29
4	573	I/O	AB33	R22	R22
4	574	I/O	AB34	M23	R23
4	575	I/O	AB35	L22	R24
4	576	I/O, LOCK1 (9)	AA30	L21	AC30
–	577	VCCINT	VCCINT	VCCINT	VCCINT
–	578	GNDINT	GND	GND	GND
4	579	I/O	AA32	L23	R25
4	580	I/O	AA33	L24	R26
4	581	I/O	AA34	N23	R27
–	582	VCC_CKLK1 (2)	AA35	AF18	W24
–	583	GND_CKLK1 (2)	Y30	AE18	V24
–	584	GND_CKLK1 (2)	Y30	AE18	V24
–	585	GNDIO	GND	GND	GND
4	586	I/O, CLKLK_FB1n (4)	Y31	AF20	AM28
4	587	CLKLK_FB1p	Y32	AE20	AL28
4	588	I/O, CLK3n (4)	Y33	M20	Y30
4	589	CLK3p	Y34	M19	W30
4	590	I/O, CLK1n (4)	Y35	P19	V30
–	591	VCCINT	VCCINT	VCCINT	VCCINT
–	592	GNDINT	GND	GND	GND
–	593	nCONFIG (5)	W32	P21	R30
–	594	CLKLK_ENA (5), (10)	W33	P16	P30
4	595	CLK1p	W34	P20	N30
–	596	MSEL1 (5)	W35	N20	K30
–	597	MSEL0 (5)	U35	N21	J30
–	598	GNDINT	GND	GND	GND
–	599	VCCINT	VCCINT	VCCINT	VCCINT
–	600	VCC_CKOUT1 (7)	U33	AF22	N24
–	601	GND_CKOUT1 (7)	U32	AE22	T24
–	602	CLKLK_OUT1p (8)	U31	AE23	AM29
3	603	I/O, CLKLK_OUT1n (4)	T35	AF23	AL29
–	604	VCC_CKLK3 (2)	T34	AC26	M24
–	605	VCCIO	VCCIO3	VCCIO3	VCCIO3
–	606	GND_CKLK3 (2)	V35	N25	P23
–	607	GND_CKLK3 (2)	T33	AC25	P24
3	608	I/O, LVDSRXINCLK1p	T32	AB25	B29
3	609	I/O, LVDSRXINCLK1n (4)	T31	AB26	A29
3	610	I/O	T30	J23	R28
3	611	I/O	R35	L19	R29
–	612	GNDINT	GND	GND	GND
–	613	VCCINT	VCCINT	VCCINT	VCCINT
3	614	I/O, LVDSRX01p	R33	AA25	AJ32
3	615	I/O, LVDSRX01n (4)	R32	AA26	AJ31
3	616	I/O, LOCK3 (9)	R31	L18	H30
3	617	I/O, LVDSRX02n (4)	R30	Y25	AH32

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
3	618	I/O, LVDSRX02p	P35	Y26	AH31
–	619	GNDIO	GND	GND	GND
3	620	I/O, LVDSRX03p	P34	W25	AE32
3	621	I/O, LVDSRX03n (4)	P33	W26	AE31
3	622	I/O	P32	J24	P22
3	623	I/O, LVDSRX04n (4)	P31	V25	AD32
3	624	I/O, LVDSRX04p	P30	V26	AD31
–	625	GNDINT	GND	GND	GND
–	626	VCCINT	VCCINT	VCCINT	VCCINT
3	627	I/O, LVDSRX05p	N34	U25	AC32
3	628	I/O, LVDSRX05n (4)	N33	U26	AC31
3	629	I/O	N32	K21	P25
3	630	I/O, LVDSRX06n (4)	N31	T25	Y32
3	631	I/O, LVDSRX06p	N30	T26	Y31
–	632	VCCIO	VCCIO3	VCCIO3	VCCIO3
3	633	I/O, LVDSRX07p	M35	R25	W32
3	634	I/O, LVDSRX07n (4)	M34	R26	W31
3	635	I/O	M33	K23	P26
3	636	I/O, LVDSRX08n (4)	M32	M25	V32
3	637	I/O, LVDSRX08p	M31	M26	V31
–	638	GNDINT	GND	GND	GND
–	639	VCCINT	VCCINT	VCCINT	VCCINT
3	640	I/O, LVDSRX09p	L35	L25	R32
3	641	I/O, LVDSRX09n (4)	L34	L26	R31
3	642	I/O	L33	K20	P27
3	643	I/O, LVDSRX10n (4)	L32	K25	P32
3	644	I/O, LVDSRX10p	L31	K26	P31
–	645	GNDIO	GND	GND	GND
3	646	I/O, LVDSRX11p	L30	J25	N32
3	647	I/O, LVDSRX11n (4)	K35	J26	N31
3	648	I/O	K34	K22	P28
3	649	I/O, LVDSRX12n (4)	K33	H25	K32
3	650	I/O, LVDSRX12p	K32	H26	K31
–	651	GNDINT	GND	GND	GND
–	652	VCCINT	VCCINT	VCCINT	VCCINT
3	653	I/O, LVDSRX13p	K30	G25	J32
3	654	I/O, LVDSRX13n (4)	J35	G26	J31
3	655	I/O	H35	K24	P29
3	656	I/O, LVDSRX14n (4)	J34	F25	H32
3	657	I/O, LVDSRX14p	J33	F26	H31
–	658	VCCIO	VCCIO3	VCCIO3	VCCIO3
3	659	I/O, LVDSRX15p	J32	E25	E32
3	660	I/O, LVDSRX15n (4)	J31	E26	E31
3	661	I/O	J30	H24	N22
3	662	I/O, LVDSRX16n (4)	G35	D25	D32
3	663	I/O, LVDSRX16p	H34	D26	D31
–	664	GNDINT	GND	GND	GND
–	665	VCCINT	VCCINT	VCCINT	VCCINT

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
–	666	GNDINT	GND	GND	GND
–	667	VCCINT	VCCINT	VCCINT	VCCINT
3	668	I/O	H33	K19	N23
3	669	I/O	–	–	N25
3	670	I/O	H32	J20	N26
3	671	I/O	–	–	N27
3	672	I/O	–	–	N28
–	673	GNDIO	GND	GND	GND
3	674	I/O	H31	G22	N29
3	675	I/O	–	–	M22
3	676	I/O	H30	H20	M23
3	677	I/O	–	–	M25
3	678	I/O	–	–	M26
–	679	GNDINT	GND	GND	GND
–	680	VCCINT	VCCINT	VCCINT	VCCINT
3	681	I/O	G34	H22	M27
3	682	I/O	–	–	M28
3	683	I/O	E35	J22	L26
3	684	I/O	–	–	L27
3	685	I/O	–	–	L28
–	686	VCCIO	VCCIO3	VCCIO3	VCCIO3
3	687	I/O	F34	G24	K26
3	688	I/O	–	–	K27
3	689	I/O	G33	H21	K28
3	690	I/O	–	–	K29
3	691	I/O	–	–	J26
–	692	GNDINT	GND	GND	GND
–	693	VCCINT	VCCINT	VCCINT	VCCINT
3	694	I/O	G32	G21	J27
3	695	I/O	–	–	J28
3	696	I/O	G31	J21	J29
3	697	I/O	–	–	H26
3	698	I/O	–	–	H27
–	699	GNDIO	GND	GND	GND
3	700	I/O	D35	F22	H28
3	701	I/O	–	–	H29
3	702	I/O	E34	G20	G27
3	703	I/O	–	–	G28
3	704	I/O	–	–	F28
–	705	GNDINT	GND	GND	GND
–	706	VCCINT	VCCINT	VCCINT	VCCINT
3	707	I/O	F33	F21	E28
3	708	I/O	–	–	E29
3	709	I/O	F32	E22	E30
3	710	I/O	–	–	D28
–	711	VCCIO	VCCIO3	VCCIO3	VCCIO3
–	712	VCCIO	VCCIO2	VCCIO2	VCCIO2
2	713	I/O	–	E23	D29

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
2	714	I/O	–	D22	D30
2	715	I/O	–	F24	C28
–	716	GNDINT	GND	GND	GND
–	717	VCCINT	VCCINT	VCCINT	VCCINT
2	718	I/O	–	E24	C29
2	719	I/O	–	H23	B28
2	720	I/O	E29	C23	A28
2	721	I/O	–	–	F27
2	722	I/O	D30	G23	E27
2	723	I/O	–	–	G26
2	724	I/O	B33	C22	F26
–	725	GNDIO	GND	GND	GND
2	726	I/O	C31	F23	E26
2	727	I/O	A34	B23	L25
2	728	I/O	B32	A23	K25
2	729	I/O	E28	E21	J25
2	730	I/O	D29	B22	H25
2	731	I/O	–	–	G25
2	732	I/O	C30	F20	F25
2	733	I/O	–	–	E25
2	734	I/O	A33	D21	D25
2	735	I/O	–	–	C25
–	736	VCCIO	VCCIO2	VCCIO2	VCCIO2
2	737	I/O	–	–	B25
2	738	I/O	B31	C21	A25
2	739	I/O	–	–	L24
2	740	I/O	E27	E20	K24
2	741	I/O	–	–	J24
2	742	I/O	A32	J19	H24
2	743	I/O	D28	A22	G24
2	744	I/O	C29	G19	F24
2	745	I/O	B30	F19	E24
2	746	I/O	A31	E19	D24
–	747	GNDIO	GND	GND	GND
2	748	I/O	D27	K18	C24
2	749	I/O	–	–	B24
2	750	I/O	E26	D20	L23
2	751	I/O	–	–	K23
2	752	I/O	C28	H18	J23
2	753	I/O	–	–	H23
2	754	I/O	–	–	G23
2	755	I/O	B29	C20	F23
2	756	I/O	–	–	E23
2	757	I/O	A30	G18	D23
–	758	VCCIO	VCCIO2	VCCIO2	VCCIO2
2	759	I/O	–	–	C23
2	760	I/O	D26	D19	B23
2	761	I/O	C27	E18	L22

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
2	762	I/O	E25	B20	K22
2	763	I/O	B28	A20	J22
2	764	I/O	A29	F18	H22
2	765	I/O	D25	C19	G22
2	766	I/O	–	–	F22
2	767	I/O	C26	E17	E22
2	768	I/O	–	–	–
2	769	I/O	B27	D18	L21
–	770	GNDIO	GND	GND	GND
–	771	GNDINT	GND	GND	GND
–	772	GNDINT	GND	GND	GND
–	773	VCCINT	VCCINT	VCCINT	VCCINT
–	774	VCCINT	VCCINT	VCCINT	VCCINT
–	775	GNDINT	–	–	–
2	776	I/O	A28	F17	K21
2	777	I/O	–	–	–
2	778	I/O	C25	C18	J21
2	779	I/O	–	–	H21
2	780	I/O	B26	G17	G21
2	781	I/O	A27	B18	F21
2	782	I/O	E23	H17	E21
2	783	I/O	D23	F16	L20
2	784	I/O	C24	D17	K20
2	785	I/O	B25	J17	J20
2	786	I/O	–	–	H20
–	787	VCCIO	VCCIO2	VCCIO2	VCCIO2
2	788	I/O	E22	E16	G20
2	789	I/O	–	–	F20
2	790	I/O	A26	G16	E20
2	791	I/O	–	–	D20
2	792	I/O	–	–	C20
2	793	I/O	C23	A18	B20
2	794	I/O	–	–	L19
2	795	I/O	B24	H16	K19
2	796	I/O	–	–	J19
2	797	I/O	D22	C17	H19
–	798	GNDIO	GND	GND	GND
2	799	I/O	A25	E15	G19
2	800	I/O	E21	D16	F19
2	801	I/O	C22	B17	E19
2	802	I/O	B23	F15	D19
2	803	I/O	A24	A17	C19
2	804	I/O	–	–	B19
2	805	I/O	A23	E14	L18
2	806	I/O	–	–	K18
2	807	I/O	D21	H15	J18
2	808	I/O	–	–	H18
–	809	VCCIO	VCCIO2	VCCIO2	VCCIO2

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
2	810	I/O	–	–	G18
2	811	I/O	C21	E13	F18
2	812	I/O	–	–	E18
2	813	I/O	E20	L14	D18
2	814	I/O	–	–	C18
2	815	I/O	B22	G15	B18
2	816	I/O	A22	K15	L17
2	817	I/O	B21	J16	K17
2	818	I/O	A21	C16	J17
2	819	I/O	D20	B16	H17
–	820	GNDIO	GND	GND	GND
2	821	I/O	C20	C15	G17
2	822	I/O	–	–	F17
2	823	I/O	B20	B15	E17
2	824	I/O	–	–	D17
2	825	I/O	A20	A15	C17
–	826	VCCIO	VCCIO2	VCCIO2	VCCIO2
–	827	TRST (5)	D19	F14	A24
–	828	NCEO (5)	C19	G14	A23
1	829	FAST1	B19	H14	A20
–	830	GNDINT	GND	GND	GND
–	831	GNDINT	GND	GND	GND
–	832	VCCINT	VCCINT	VCCINT	VCCINT
–	833	VCCINT	VCCINT	VCCINT	VCCINT
–	834	VCCIO	VCCIO1	VCCIO1	VCCIO1
1	835	FAST2	B17	F13	A19
–	836	TDO (5)	C17	G13	A18
–	837	GNDINT	GND	GND	–
1	838	I/O	A16	C14	C16
1	839	I/O	–	–	D16
1	840	I/O	B16	B14	E16
1	841	I/O	–	–	F16
1	842	I/O, INITDONE (3)	C16	J15	A15
–	843	GNDIO	GND	GND	GND
1	844	I/O	D16	C12	G16
1	845	I/O	A15	B13	H16
1	846	I/O	B15	C11	J16
1	847	I/O, RDYNBSY (1)	A14	J14	A14
1	848	I/O	B14	D15	K16
1	849	I/O	–	–	L16
1	850	I/O	E16	D14	B15
1	851	I/O	–	–	C15
1	852	I/O, CLKUSR (1)	C15	K14	A13
1	853	I/O	–	–	D15
–	854	VCCIO	VCCIO1	VCCIO1	VCCIO1
1	855	I/O	–	–	E15
1	856	I/O	D15	A12	F15
1	857	I/O	–	–	G15

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
1	858	I/O	A13	D13	H15
1	859	I/O	–	–	J15
1	860	I/O	A12	B11	K15
1	861	I/O	B13	B12	L15
1	862	I/O	C14	H13	B14
1	863	I/O	E15	F12	C14
1	864	I/O	A11	A11	D14
–	865	GNDIO	GND	GND	GND
1	866	I/O	D14	E12	E14
1	867	I/O	–	–	F14
1	868	I/O	B12	A10	G14
1	869	I/O	–	–	H14
1	870	I/O, DATA1 (1)	C13	K13	A10
1	871	I/O	–	–	J14
1	872	I/O	–	–	K14
1	873	I/O	A10	D12	L14
1	874	I/O	–	–	B13
1	875	I/O	E14	D11	C13
–	876	VCCIO	VCCIO1	VCCIO1	VCCIO1
1	877	I/O	–	–	D13
1	878	I/O	B11	E11	E13
1	879	I/O	C12	B10	F13
1	880	I/O	D13	C10	G13
1	881	I/O	E13	J13	H13
1	882	I/O	A9	D10	J13
1	883	I/O	B10	H12	K13
1	884	I/O	–	–	L13
1	885	I/O	C11	E10	E12
1	886	I/O	–	–	–
1	887	I/O, DATA2 (1)	A8	J12	A9
–	888	GNDIO	GND	GND	GND
–	889	GNDINT	GND	GND	GND
–	890	GNDINT	GND	GND	GND
–	891	VCCINT	VCCINT	VCCINT	VCCINT
–	892	VCCINT	VCCINT	VCCINT	VCCINT
1	893	I/O	B9	F11	F12
1	894	I/O	–	–	–
1	895	I/O	C10	B9	G12
1	896	I/O	–	–	H12
1	897	I/O	D11	G12	J12
1	898	I/O	A7	C9	K12
1	899	I/O	B8	G11	L12
1	900	I/O	E11	E9	E11
1	901	I/O	C9	F9	F11
1	902	I/O	D10	D9	G11
1	903	I/O	–	–	H11
–	904	VCCIO	VCCIO1	VCCIO1	VCCIO1
1	905	I/O	A6	K12	J11

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
1	906	I/O	–	–	K11
1	907	I/O, DATA3 (1)	B7	F10	A8
1	908	I/O	–	–	L11
1	909	I/O	–	–	B10
1	910	I/O	C8	A9	C10
1	911	I/O	–	–	D10
1	912	I/O	E10	H11	E10
1	913	I/O	–	–	F10
1	914	I/O	D9	D8	G10
–	915	GNDIO	GND	GND	GND
1	916	I/O	A5	E8	H10
1	917	I/O	B6	C8	J10
1	918	I/O	C7	F8	K10
1	919	I/O	D8	E7	L10
1	920	I/O	A4	G10	B9
1	921	I/O	–	–	C9
1	922	I/O	E9	C7	D9
1	923	I/O	–	–	E9
1	924	I/O, DATA4 (1)	B5	G9	B5
1	925	I/O	–	–	F9
–	926	VCCIO	VCCIO1	VCCIO1	VCCIO1
1	927	I/O	–	–	G9
1	928	I/O	A3	H10	H9
1	929	I/O	–	–	J9
1	930	I/O	C6	B7	K9
1	931	I/O	–	–	L9
1	932	I/O	D7	J11	B8
1	933	I/O	E8	D7	C8
1	934	I/O	B4	D6	D8
1	935	I/O	A2	A7	E8
1	936	I/O	C5	F7	F8
–	937	GNDIO	GND	GND	GND
1	938	I/O	B3	E6	G8
1	939	I/O	–	–	H8
1	940	I/O	D6	C5	E7
1	941	I/O	–	–	F7
1	942	I/O, DATA5 (1)	E7	F6	A5
1	943	–	–	–	–

Pin Name	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
MSEL0 (5)	U35	N21	J30
MSEL1 (5)	W35	N20	K30
nSTATUS (5)	AN17	AA13	AM14
nCONFIG (5)	W32	P21	R30
DCLK (5)	U3	N7	W3
CONF_DONE (5)	AM17	AA12	AM13
INIT_DONE (3)	C16	J15	A15
nCE (5)	U1	P6	AC3
nCEO (5)	C19	G14	A23
nWS (1)	M1	P9	C4
nRS (1)	N1	N10	D4
nCS (1)	P2	M9	D3
CS (1)	R2	T6	E3
RDYnBSY (1)	A14	J14	A14
CLKUSR (1)	C15	K14	A13
DATA7 (1)	M6	M10	B4
DATA6 (1)	L6	L8	A4
DATA5 (1)	E7	F6	A5
DATA4 (1)	B5	G9	B5
DATA3 (1)	B7	F10	A8
DATA2 (1)	A8	J12	A9
DATA1 (1)	C13	K13	A10
DATA0 (5), (6)	U4	N6	V3
TDI (5)	W1	P7	AD3
TDO (5)	C17	G13	A18
TCK (5)	AN19	AA14	AM19
TMS (5)	AM19	AA15	AM20
TRST (5)	D19	F14	A24
Dedicated Fast I/Os	AP19, AP17, B17, B19	Y14, Y13, F13, H14	AM18, AM15, A19, A20
CLK1p	W34	P20	N30
CLK2p	U2	N8	Y3
CLK3p	Y34	M19	W30
CLK4p	T2	R6	P3
LOCK1 (9)	AA30	L21	AC30
LOCK2 (9)	AB6	U6	AK4
LOCK3 (9)	R31	L18	H30
LOCK4 (9)	AC6	W7	AK5
CLKLK_ENA (5), (10)	W33	P16	P30
CLKLK_OUT1p (8)	U31	AE23	AM29
CLKLK_OUT2p (8)	Y3	T7	AH3
CLKLK_FB1p	Y32	AE20	AL28
CLKLK_FB2p	T4	U8	K3
DEV_CLRn (3)	T6	R9	H3
DEV_OE (3)	Y5	R8	AE3

Pin Name	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
VCCINT	A17, A19, AA31, AA4, AC3, AC32, AE2, AE33, AG1, AH31, AH35, AH4, AK33, AL12, AL2, AL24, AM12, AM24, AR17, AR19, D12, D24, E12, E24, F3, F35, G30, H1, H5, K31, L3, M30, N35, N4, R34, R5, U34, U5, W3, W31	A3, A24, B3, B8, B19, B24, C1, C2, C25, C26, D3, D24, K11, L10, L15, M13, M16, N2, N12, P15, P24, P25, R11, R14, T12, T17, U9, U16, AC3, AC24, AD1, AD2, AD25, AD26, AE3, AE8, AE19, AE24, AF3, AF24	A2, B1, F1, F2, L1, L2, U1, U2, U3, AB1, AB2, AG1, AG2, AL1, AM2, AL6, AM6, AL11, AM11, AL17, AM17, AL22, AM22, AL27, AM27, AM31, AL32, AG31, AG32, AB31, AB32, T30, T31, T32, L31, L32, F31, F32, B32, A31, A27, B27, A22, B22, A16, B16, A11, B11, A6, B6
VCCIO1	C4, D5, E17	A6, J10, L12	A12, B12, A7, B7, A3
VCCIO2	E19, D31, C32	A13, K16, M14, A16	A30, A26, B26, A21, B21
VCCIO3	F30, F31, U30	A21, L17, N15	M31, M32, G31, G32, C32
VCCIO4	W30, AL31, AL32	N24, R16, U18	AK32, AF31, AF32, AA31, AA32
VCCIO5	AN32, AN33, AL19	T15, V17, AF21	AL21, AM21, AL26, AM26, AM30
VCCIO6	AL17, AM5, AN4	R13, U11, V10, AF13	AM3, AL7, AM7, AL12, AM12
VCCIO7	AL3, AL4, W6	P12, T10, AF6	AA1, AA2, AF1, AF2, AK1
VCCIO8	U6, E3, E4	K9, M11, N3	C1, G1, G2, M1, M2
VCC_CKLK1 (2)	AA35	AF18	W24
VCC_CKLK2 (2)	W4	N11	Y9
VCC_CKLK3 (2)	T34	AC26	M24
VCC_CKLK4 (2)	R4	P10	P9
VCC_CKOUT1 (7)	U33	AF22	N24
VCC_CKOUT2 (7)	Y1	V7	AA9
GND	A1, A18, A35, AK18, AL18, AL30, AL5, AL6, AM18, AM2, AM3, AM31, AM32, AM33, AM34, AM4, AN1, AN18, AN2, AN3, AN34, AN35, AP1, AP18, AP2, AP34, AP35, AR1, AR18, AR35, B1, B18, B2, B34, B35, C18, C2, C3, C33, C34, C35, D18, D17, D2, D3, D32, D33, D34, D4, E18, E30, E31, E32, E33, E5, E6, F18, V1, V2, V3, V30, V31, V32, V33, V34, V4, V5, V6	A2, A8, A14, A19, A25, B1, B2, B6, B21, B25, B26, C3, C13, C24, D4, D23, H8, H19, J9, J18, K10, K17, L11, L13, L16, M12 M15, N1, N4, N13, N14, N26, P1, P2, P3, P13, P14, P23, P26, R12, R15, T11, T16, U10, U17, V9, V18, W8, W19, AC4, AC23, AD3, AD13, AD24, AE1, AE2, AE6, AE21, AE25, AE26, AF2, AF8, AF14, AF19, AF25, AF15	B2, B3, C2, C3, F3, F4, G3, G4, L3, L4, M3, M4, T1, T2, T3, AA3, AA4, AB3, AB4, AF3, AF4, AG3, AG4, AK2, AK3, AL2, AL3, AJ6, AJ7, AK6, AK7, AJ11, AJ12, AK11, AK12, AL16, AM16, AJ21, AJ22, AK21, AK22, AJ26, AJ27, AK26, AK27, AK30, AK31, AL30, AL31, AG29, AG30, AF29, AF30, AB29, AB30, AA29, AA30, U30, U31, U32, M29, M30, L29, L30, G29, G30, F29, F30, C30, C31, B30, B31, C26, C27, D26, D27, C21, C22, D21, D22, A17, B17, C11, C12, D11, D12, C6, C7, D6, D7
GND_CKLK1 (2)	Y30	AE18	V24
GND_CKLK2 (2)	W2	P11	V9
GND_CKLK3 (2)	T33, V35	AC25, N25	P24, P23
GND_CKLK4 (2)	R3	R10	T9
GND_CKOUT1 (7)	U32	AE22	T24
GND_CKOUT2 (7)	Y2	V6	W9

Pin Name	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
No Connect (N.C.)			M12, M13, M14, M15, M16, M17, M18, M19, M20, M21, N12, N13, N14, N15, N16, N17, N18, N19, N20, N21, P12, P13, P14, P15, P16, P17, P18, P19, P20, P21, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, T12, T13, T14, T15, T16, T17, T18, T19, T20, T21, U12, U13, U14, U15, U16, U17, U18, U19, U20, U21, V12, V13, V14, V15, V16, V17, V18, V19, V20, V21, W12, W13, W14, W15, W16, W17, W18, W19, W20, W21, Y12, Y13, Y14, Y15, Y16, Y17, Y18, Y19, Y20, Y21, AA12, AA13, AA14, AA15, AA16, AA17, AA18, AA19, AA20, AA21
Total User I/O Pins (11)	488	508	708

Notes:

(1) This pin can be used as a user I/O pin after configuration.

(2) This pin is the power or ground for the ClockLock and ClockBoost circuitry. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device. VCC_CKLK has the same voltage specifications as the VCCINT and should be connected to a 1.8-V power supply. If the ClockLock or ClockBoost circuitry is not used, this power or ground pin should be connected to VCCINT or GNDINT, respectively.

(3) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.

(4) This pin is the complementary signal for the LVDS pair on dedicated inputs and outputs that can be configured for the LVDS standard. If not used for the LVDS pair, these pins are regular I/O pins. Pins with the "n" suffix carry the negative signal for the LVDS channel. Pins with a "p" suffix carry the positive signal for the LVDS channel.

(5) This pin is a dedicated pin; it is not available as a user I/O pin.

(6) This pin is tri-stated in user mode.

(7) This pin is the power or ground for the external output of a PLL. These pins should be set to the VCCIO level/standard desired for the external clock ouput. To ensure noise resistance, the power and ground supply to the PLL external output should be isolated from the power and ground to the rest of the VCCIO and GNDIO pins. If the PLL or external output is not used, this power or ground pin should be connected to VCCIO or GNDIO, respectively.

(8) The CLKLK_OUT pin is powered by the VCC_CKOUT and GND_CKOUT pins.

(9) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry is locked to the incoming clock and generates an internal clock, LOCK is driven high. LOCK remains high if a periodic clock stops clocking. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.

(10) This pin is the active high enable pin for all of the PLL circuits in the device. When de-asserted, all PLLs are reset to their default, unlocked state and will stop clocking. Once re-asserted, the PLLs will lock again and start clocking. If this pin function is not needed, the pin should be connected to VCCINT.

(11) The user I/O pin count includes dedicated inputs and dedicated clock inputs. It does not include the dedicated clock feedback and output pins.

Pin Name (1)	**144-Pin TQFP**	**208-Pin PQFP** (2)	**240-Pin PQFP** (3)	**324-Pin FineLine BGA**	**356-Pin BGA**
MSEL0 (4)	18	25	29	J17	P1
MSEL1 (4)	19	26	30	J16	P2
nSTATUS (4)	57	82	92	U9	AF15
nCONFIG (4)	22	29	33	K17	R1
DCLK (4)	93	132	152	J3	N25
CONF_DONE (4)	58	83	93	U8	AE15
INIT_DONE (5)	121	178	206	E11	A16
nCE (4)	91	130	150	K2	P26
nCEO (4)	128	185	213	C10	A12
nWS (6)	103	145	164	K5	H22
nRS (6)	102	142	161	J6	H24
nCS (6)	101	141	160	H5	J24
CS (6)	98	138	157	M2	K25
RDYnBSY (6)	120	177	205	E10	B16
CLKUSR (6)	119	176	204	F10	C16
DATA7 (6)	104	146	166	H6	G23
DATA6 (6)	105	150	169	G4	F24
DATA5 (6)	109	157	181	B2	C24
DATA4 (6)	111	160	185	C5	A25
DATA3 (6)	112	163	189	B6	B22
DATA2 (6)	115	168	195	E8	B20
DATA1 (6)	117	173	200	F9	B18
DATA0 (4), (7)	94	133	153	J2	M26
TDI (4)	90	129	149	K3	P25
TDO (4)	123	180	208	C9	B15
TCK (4)	52	76	87	U10	AE12
TMS (4)	51	75	86	U11	AF11
TRST (4)	129	186	214	B10	B12
Dedicated Inputs	56, 53, 124, 127	81, 77, 181, 184	91, 88, 209, 212	B9, D10, T9, T10	A13, A15, AE14, AF12
LOCK (8)	80	119	138	N2	P3
CLK2 (9)	92	131	151	J4	N26
CLK1	20	27	31	K16	T24
DEV_CLRn (5)	97	137	156	L5	L23
DEV_OE (5)	84	124	143	L4	R26
VCCINT	125, 108, 86, 73, 55, 36, 21, 16, 1	182, 156, 126, 105, 79, 52, 28, 23, 1	1, 27, 32, 60, 90, 122, 145, 179, 210	F7, G6, G11, H9, H12, J8, K11, K12, L7, L10, M8, M13, N5, N12	A14, AB25, AB3, AF13, AF14, B14, E23, E1, H1, J23, L1, M25, P4, R2, T22, U4, Y26
VCCIO	144, 116, 89, 61, 28	136, 86, 80, 53, 8, 208, 189, 172	12, 45, 67, 97, 120, 148, 177, 199, 229	E6, F5, F12, G8, G13, H7, H10, J11, K8, L9, L12, M6, M11, N7, N14, P6, P13	C26, M22, P22, AD26, AF26, AD14, AD12, AF1, AD1, P5, M5, C1, A1, C12, C14, A26
VCC_CKLK (10)	85	125	144	J7	P23

Pin Name (1)	**144-Pin TQFP**	**208-Pin PQFP** (2)	**240-Pin PQFP** (3)	**324-Pin FineLine BGA**	**356-Pin BGA**
GNDINT	126, 87, 77, 74, 54, 34, 17, 4	183, 143, 127, 118, 78, 39, 24, 16	19, 28, 42, 89, 137, 146, 162, 211	G9, D4, D15, E5, E14, F6, F13, G7, G12, H8, H11, J9, J10, K9, K10, L8, L11, M7, M12, N6, N13, P5, P14, R4, R15	AB4, AB5, AC3, AC22, AC23, AC24, AD2, AD13, AD25, AE1, AE13, AE26, B1, B13, B26, C2, C13, C25, D3, D4, D22, D23, D24, E5, N3, N4, N5, N22, N23, N24
GNDIO (11)	134, 106, 72, 42, 12	199, 169, 149, 114, 95, 64, 43, 10	26, 56, 78, 108, 132, 165, 188, 218, 240	–	–
GND_CKLK (10)	88	128	147	K7	P24
No Connect (N.C.)	–	–	–	–	AA26, AA25, AA3, AA2, AA1, AA24, AA23, AB26, AB2, AB1, AB24, AB23, AB22, AC26, AC25, AC2, AC1, D2, D1, E4, E3, E2, J25, K26, K23
Total User I/O Pins (12)	101	159	189	252	252

Notes:

(1) All pins that are not listed are user I/O pins.

(2) EP20K100 devices in 208-pin PQFP packages are pin-compatible with EP20K200 devices in the same package if pins 154, 148, 121, 109, 48, 36, 11, and 3 are tri-stated and connected to VCCINT, and if pins 153, 147, 110, 47, 35, 12, and 4 are tristated and connected to GNDINT.

(3) EP20K100 devices in 240-pin PQFP packages are pin-compatible with EP20K200 devices in the same package if pins 176, 168, 140, 127, 52, 39, 14, and 5 are tri-stated and connected to VCCINT, and if pins 175, 167, 128, 51, 38, 15, and 6 are tri-stated and connected to GNDINT.

(4) This pin is a dedicated pin; it is not available as a user I/O pin.

(5) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.

(6) This pin can be used as a user I/O pin after configuration.

(7) This pin is tri-stated in user mode.

(8) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry is locked to the incoming clock and generates an internal clock, LOCK is driven high. LOCK remains high if a periodic clock stops clocking. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.

(9) This pin drives the ClockLock and ClockBoost circuitry.

(10) This pin is the power or ground for the ClockLock and ClockBoost circuitry. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device. VCC_CKLK has the same voltage specifications as the VCCINT and should be connected to a 2.5-V power supply. If the ClockLock or ClockBoost circuitry is not used, this power or ground pin should be connected to VCCINT or GNDINT, respectively.

(11) GNDIO and GNDINT are connected together in BGA packages.

(12) The user I/O pin count includes dedicated inputs, dedicated clock inputs, and all I/O pins.

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	144-Pin TQFP (1)	208-Pin PQFP (1)	240-Pin PQFP (1)	144-Pin FineLine BGA	324-Pin FineLine BGA	356-Pin BGA
8	1	I/O	–	–	180	–	A1	E22
8	2	I/O	–	155	178	–	B1	F22
8	3	I/O	–	–	–	–	C1	D25
–	4	VCCIO	VCCIO8	VCCIO8	VCCIO8	VCCIO8	–	VCCIO8
8	5	I/O	–	–	–	–	C4	E24
–	6	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
8	7	I/O	–	154	176	–	C2	F23
8	8	I/O	–	–	175	–	D1	D26
8	9	I/O	–	153	174	–	C3	G22
8	10	I/O	–	–	173	–	D3	E25
8	11	I/O	–	152	172	–	D2	E26
–	12	VCCIO	VCCIO8	VCCIO8	VCCIO8	VCCIO8	VCCIO8	VCCIO8
8	13	I/O	–	–	171	–	F3	F25
8	14	I/O	–	–	–	–	E1	G24
8	15	I/O	–	151	170	–	D5	F26
8	16	I/O	–	–	–	–	E4	H23
8	17	I/O, DATA6 (2)	105	150	169	B2	G4	F24
–	18	GNDINT	GND	GND	GND	GND	GND	GND
8	19	I/O	–	–	–	–	F1	G25
8	20	I/O	–	148	168	–	E2	J22
8	21	I/O	–	147	167	–	G2	G26
8	22	I/O	–	–	–	–	E3	H25
8	23	I/O, DATA7 (2)	104	146	166	C1	H6	G23
–	24	GNDIO	GND	GND	GND	GND	GND	GND
8	25	I/O, nWS (2)	103	145	164	C2	K5	H22
8	26	I/O	–	–	–	–	F4	H26
8	27	I/O	–	144	163	–	F2	K22
8	28	I/O, nRS (2)	102	142	161	D2	J6	H24
8	29	I/O, nCS (2)	101	141	160	D3	H5	J24
–	30	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
–	31	VCC_CKLK4 (3)	100	140	159	D4	K6	K24
–	32	GND_CKLK4 (3)	99	139	158	E2	L6	L22
–	33	GND_CKLK4 (3)	99	139	158	E2	L6	L22
8	34	I/O	–	–	–	–	J1	J26
8	35	I/O, CS (2)	98	138	157	E3	M2	K25
8	36	I/O, DEV_CLRn (4)	97	137	156	E4	L5	L23
–	37	VCCIO	VCCIO8	VCCIO8	VCCIO8	VCCIO8	VCCIO8	VCCIO8
8	38	I/O, CLKLK_FB2n (5)	–	–	–	F5	M4	L24
8	39	CLKLK_FB2p	96	135	155	F4	N4	L25
8	40	I/O, CLK4n (5)	–	–	–	F3	L3	L26
8	41	CLK4p	95	134	154	F2	L2	M23
8	42	I/O, CLK2n (5)	–	–	–	G4	J5	M24
–	43	DATA0 (6), (11)	94	133	153	G3	J2	M26
–	44	DCLK (6)	93	132	152	G2	J3	N25
8	45	CLK2p	92	131	151	G7	J4	N26
–	46	nCE (6)	91	130	150	H5	K2	P26

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	144-Pin TQFP (1)	208-Pin PQFP (1)	240-Pin PQFP (1)	144-Pin FineLine BGA	324-Pin FineLine BGA	356-Pin BGA
–	47	TDI (6)	90	129	149	H2	K3	P25
–	48	VCCIO	VCCIO7	VCCIO7	VCCIO7	VCCIO7	VCCIO7	VCCIO7
–	49	GND_CKLK2 (3)	88	128	147	G5	K7	P24
–	50	GND_CKLK2 (3)	88	128	147	G5	K7	P24
–	51	GNDINT	GND	GND	GND	GND	GND	GND
–	52	VCC_CKLK2 (3)	85	125	144	G6	J7	P23
7	53	I/O, DEV_OE (4)	84	124	143	J3	L4	R26
–	54	VCC_CKOUT2 (7)	83	123	142	H4	P3	R25
–	55	GND_CKOUT2 (7)	82	122	141	H3	P2	R24
7	56	I/O	–	–	–	–	H4	T26
7	57	I/O	–	121	140	–	H2	T25
–	58	GNDIO	GND	GND	GND	GND	GND	GND
–	59	CLKLK_OUT2p (8)	81	120	139	J2	M3	R23
7	60	I/O, CLKLK_OUT2n (5)	–	–	–	K2	N3	R22
7	61	I/O, LOCK2 (9)	80	119	138	K3	N2	T24
7	62	I/O	–	–	–	–	G3	T23
7	63	I/O	79	117	136	L1	G5	U26
–	64	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
7	65	I/O, LOCK4 (9)	78	116	135	L2	R3	V25
7	66	I/O	–	–	–	–	H3	U25
7	67	I/O	–	–	134	–	G1	U24
7	68	I/O	–	–	–	–	K4	U23
7	69	I/O	–	–	133	–	H1	U22
–	70	VCCIO	VCCIO7	VCCIO7	VCCIO7	VCCIO7	VCCIO7	VCCIO7
7	71	I/O	–	–	–	–	K1	V26
7	72	I/O	–	–	131	–	L1	V24
7	73	I/O	–	–	130	–	M1	W26
7	74	I/O	–	113	129	–	N1	V23
7	75	I/O	–	112	128	–	R1	W25
–	76	GNDINT	GND	GND	GND	GND	GND	GND
7	77	I/O	76	111	127	L3	R2	W24
7	78	I/O	–	–	–	–	P1	V22
7	79	I/O	75	110	126	J4	T1	W23
7	80	I/O	–	–	–	–	V1	Y25
7	81	I/O	–	109	125	–	U1	W22
–	82	GNDIO	GND	GND	GND	GND	GND	GND
–	83	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
7	84	I/O	–	108	124	–	T2	Y24
7	85	I/O	–	–	–	–	U2	Y23
7	86	I/O	–	107	123	–	U3	Y22
7	87	I/O	–	106	121	–	V2	AA22
–	88	VCCIO	VCCIO7	VCCIO7	VCCIO7	VCCIO7	VCCIO7	VCCIO7
–	89	VCCIO	VCCIO6	VCCIO6	VCCIO6	VCCIO6	VCCIO6	VCCIO6

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	144-Pin TQFP (1)	208-Pin PQFP (1)	240-Pin PQFP (1)	144-Pin FineLine BGA	324-Pin FineLine BGA	356-Pin BGA
6	90	I/O	71	104	119	K4	V3	AD24
6	91	I/O	–	–	118	–	T3	AE25
6	92	I/O	–	103	117	–	V4	AD23
6	93	I/O	70	102	116	L4	P4	AE24
6	94	I/O	–	–	–	–	M5	AF25
6	95	I/O	69	101	115	J5	U5	AF24
6	96	I/O	–	–	–	–	U4	AD22
6	97	I/O	68	100	114	H6	T4	AE23
6	98	I/O	–	99	113	–	T5	AF23
6	99	I/O	–	–	112	–	R5	AE22
–	100	GNDIO	GND	GND	GND	GND	GND	GND
6	101	I/O	67	98	111	K5	V5	AD21
6	102	I/O	–	97	110	–	R6	AF22
6	103	I/O	66	96	109	J6	T6	AE21
6	104	I/O	–	–	–	–	U6	AD20
6	105	I/O	65	94	107	L5	V7	AF21
6	106	I/O	–	–	106	–	P7	AE20
6	107	I/O	–	93	105	–	V6	AD19
6	108	I/O	–	–	104	–	U7	AF20
6	109	I/O	64	92	103	K6	T7	AE19
6	110	I/O	–	–	–	–	R7	AD18
–	111	VCCIO	VCCIO6	VCCIO6	VCCIO6	VCCIO6	VCCIO6	VCCIO6
6	112	I/O	63	91	102	L6	P8	AF19
6	113	I/O	–	90	101	–	R8	AE18
6	114	I/O	–	–	–	–	T8	AF18
6	115	I/O	62	89	100	–	M9	AD17
6	116	I/O	–	88	99	–	R10	AE17
6	117	I/O	–	87	98	–	V8	AF17
–	118	VCCIO	VCCIO6	VCCIO6	VCCIO6	VCCIO6	–	VCCIO6
6	119	I/O	60	85	96	–	N9	AD16
6	120	I/O	59	84	95	–	N8	AE16
6	121	I/O	–	–	–	–	R9	AF16
6	122	I/O	–	–	94	–	P9	AD15
–	123	CONF_DONE (6)	58	83	93	M3	U8	AE15
–	124	nSTATUS (6)	57	82	92	M4	U9	AF15
5	125	FAST4	56	81	91	M5	T9	AE14
–	126	VCCIO	VCCIO5	VCCIO5	VCCIO5	VCCIO6	–	VCCIO5
–	127	GNDINT	GND	GND	GND	GND	GND	GND
–	128	GNDINT	–	–	–	–	–	–
–	129	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
–	130	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
–	131	GNDINT	–	–	–	–	–	–
–	132	GNDINT	GND	GND	GND	GND	GND	GND
–	133	GNDIO	GND	GND	GND	GND	GND	GND
5	134	FAST3	53	77	88	M8	T10	AF12
–	135	TCK (6)	52	76	87	M9	U10	AE12
–	136	TMS (6)	51	75	86	M10	U11	AF11

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	144-Pin TQFP (1)	208-Pin PQFP (1)	240-Pin PQFP (1)	144-Pin FineLine BGA	324-Pin FineLine BGA	356-Pin BGA
5	137	I/O	50	74	85	L7	V9	AE11
5	138	I/O	–	73	84	–	P10	AD11
5	139	I/O	–	–	83	–	V10	AF10
5	140	I/O	49	72	82	L8	T11	AE10
5	141	I/O	–	–	–	–	N10	AD10
5	142	I/O	48	71	81	K7	P11	AF9
5	143	I/O	–	–	80	–	V11	AE9
5	144	I/O	47	70	79	J7	R11	AF8
5	145	I/O	–	69	77	–	V12	AD9
5	146	I/O	46	68	76	K8	M10	AE8
–	147	VCCIO	VCCIO5	VCCIO5	VCCIO5	VCCIO5	VCCIO5	VCCIO5
5	148	I/O	–	67	75	–	U12	AF7
5	149	I/O	–	–	–	–	T12	AD8
5	150	I/O	–	66	74	–	R12	AE7
5	151	I/O	44	65	73	H7	N11	AF6
5	152	I/O	–	–	–	–	V13	AD7
5	153	I/O	–	63	72	–	P12	AE6
5	154	I/O	43	62	71	L9	U13	AF5
5	155	I/O	–	–	70	–	V14	AD6
5	156	I/O	–	61	69	–	T13	AE5
5	157	I/O	41	60	68	J8	U14	AF4
–	158	GNDIO	GND	GND	GND	GND	GND	GND
–	159	VCCIO	VCCIO5	VCCIO5	VCCIO5	VCCIO5	–	VCCIO5
5	160	I/O	40	59	66	K9	R13	AF3
5	161	I/O	–	–	–	–	T14	AE4
5	162	I/O	–	58	65	–	R14	AD5
5	163	I/O	–	–	–	–	U15	AF2
5	164	I/O	39	57	64	L10	T15	AE3
5	165	I/O	–	–	–	–	R16	AD4
5	166	I/O	38	56	63	H8	T16	AC5
5	167	I/O	–	55	62	–	V16	AE2
5	168	I/O	–	–	–	–	V15	AD3
5	169	I/O	37	54	61	K10	U16	AC4
–	170	VCCIO	VCCIO5	VCCIO5	VCCIO5	VCCIO5	VCCIO5	VCCIO5
–	171	VCCIO	VCCIO4	VCCIO4	VCCIO4	VCCIO4	VCCIO4	VCCIO4
4	172	I/O	–	51	59	–	U17	AA5
4	173	I/O	35	50	58	L12	T18	AA4
4	174	I/O	–	–	–	–	V17	Y5
4	175	I/O	–	49	57	–	N15	Y4
–	176	GNDINT	GND	GND	GND	GND	GND	GND
–	177	GNDIO	GND	GND	GND	GND	GND	GND
4	178	I/O	–	48	55	–	V18	W5
4	179	I/O	–	–	54	–	P15	Y3
4	180	I/O	33	47	53	L11	M14	Y2
4	181	I/O	–	–	52	–	R17	W4
4	182	I/O	32	46	51	K11	P16	Y1
–	183	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	144-Pin TQFP (1)	208-Pin PQFP (1)	240-Pin PQFP (1)	144-Pin FineLine BGA	324-Pin FineLine BGA	356-Pin BGA
4	184	I/O	31	45	50	J10	P17	W3
4	185	I/O	–	–	49	–	T17	V5
4	186	I/O	30	44	48	J11	R18	W2
4	187	I/O	–	–	47	–	U18	V4
4	188	I/O	29	–	46	–	N16	W1
–	189	VCCIO	VCCIO4	VCCIO4	VCCIO4	VCCIO4	VCCIO4	VCCIO4
4	190	I/O	27	41	44	–	L13	V3
4	191	I/O	–	–	–	–	M15	U5
4	192	I/O	26	40	43	J9	N17	V2
4	193	I/O	–	38	41	–	K13	V1
4	194	I/O	–	37	40	–	L14	U3
–	195	GNDINT	GND	GND	GND	GND	GND	GND
4	196	I/O	–	36	39	–	M16	U2
4	197	I/O	–	35	38	–	J12	T5
4	198	I/O	25	34	37	H10	P18	U1
4	199	I/O	–	–	–	–	L15	T4
4	200	I/O	24	33	36	H11	K14	T3
–	201	GNDIO	GND	GND	GND	GND	GND	GND
4	202	I/O	–	–	–	–	J13	T2
4	203	I/O	–	32	35	–	M17	R5
4	204	I/O, CLK3n (5)	–	–	–	H9	H16	T1
4	205	CLK3p	23	31	34	G8	H15	R4
4	206	I/O, CLK1n (5)	–	30	–	G11	K15	R3
–	207	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
–	208	nCONFIG (6)	22	29	33	G10	K17	R1
–	209	CLKLK_ENA (6), (10)	21	28	32	G9	K12	P4
4	210	CLK1p	20	27	31	F9	K16	P3
–	211	MSEL1 (6)	19	26	30	F10	J16	P2
–	212	MSEL0 (6)	18	25	29	F11	J17	P1
3	213	I/O	–	–	–	–	L17	N1
3	214	I/O	–	–	–	–	N18	N2
3	215	I/O	15	22	25	F8	L16	M1
3	216	I/O	–	–	–	–	K18	M2
3	217	I/O	–	–	–	–	J14	M3
–	218	VCCIO	VCCIO3	VCCIO3	VCCIO3	VCCIO3	VCCIO3	VCCIO3
3	219	I/O	14	21	24	F7	J15	M4
3	220	I/O	–	–	–	–	J18	L2
3	221	I/O	13	20	23	E9	G16	L3
3	222	I/O	–	–	–	–	H13	K1
3	223	I/O	–	19	22	–	M18	L4
–	224	GNDINT	GND	GND	GND	GND	GND	GND
3	225	I/O	–	18	21	–	H14	K2
3	226	I/O	–	–	–	–	H17	L5
3	227	I/O	11	17	20	E10	H18	K3
3	228	I/O	–	15	18	–	L18	J1
3	229	I/O	10	14	17	E11	G18	K4

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	144-Pin TQFP (1)	208-Pin PQFP (1)	240-Pin PQFP (1)	144-Pin FineLine BGA	324-Pin FineLine BGA	356-Pin BGA
–	230	GNDIO	GND	GND	GND	GND	GND	GND
3	231	I/O	–	–	16	–	G17	J2
3	232	I/O	–	–	15	–	G15	J3
3	233	I/O	9	13	14	E8	G14	K5
3	234	I/O	–	–	–	–	F17	H2
3	235	I/O	8	12	13	D10	F16	J4
–	236	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
–	237	VCCIO	VCCIO3	VCCIO3	VCCIO3	VCCIO3	VCCIO3	VCCIO3
3	238	I/O	–	–	11	–	F18	G1
3	239	I/O	–	–	–	–	F15	H3
3	240	I/O	7	11	10	D11	E16	J5
3	241	I/O	–	–	–	–	C18	G2
3	242	I/O	6	9	9	C10	D16	H4
–	243	VCCIO	VCCIO3	VCCIO3	VCCIO3	VCCIO3	VCCIO3	VCCIO3
3	244	I/O	–	–	8	–	D18	F1
3	245	I/O	–	7	7	–	E18	G3
3	246	I/O	–	6	6	–	D17	H5
3	247	I/O	–	–	–	–	C17	F2
3	248	I/O	–	5	5	–	E17	G4
–	249	GNDINT	GND	GND	GND	GND	GND	GND
3	250	I/O	3	4	4	C11	B18	F3
3	251	I/O	–	–	–	–	C16	G5
3	252	I/O	2	3	3	C12	B17	F4
3	253	I/O	–	2	2	–	A18	F5
–	254	VCCIO	VCCIO3	VCCIO3	VCCIO3	VCCIO2	VCCIO2	VCCIO2
–	255	GNDIO	GND	GND	GND	GND	GND	GND
2	256	I/O	143	207	239	B11	A17	C3
2	257	I/O	–	–	238	–	B16	B2
2	258	I/O	142	206	237	D9	A16	D5
2	259	I/O	–	–	–	–	E15	C4
2	260	I/O	–	205	236	–	C15	B3
2	261	I/O	–	–	–	–	B15	A2
2	262	I/O	141	204	235	C9	A15	C5
2	263	I/O	–	–	–	–	F14	B4
2	264	I/O	–	203	234	–	D14	A3
2	265	I/O	140	202	233	B10	C14	A4
–	266	VCCIO	VCCIO2	VCCIO2	VCCIO2	VCCIO2	VCCIO2	VCCIO2
2	267	I/O	139	201	232	D8	A14	B5
2	268	I/O	–	200	231	–	B14	C6
2	269	I/O	138	198	230	C8	A13	A5
2	270	I/O	–	–	–	–	B13	B6
–	271	VCCIO	VCCIO2	VCCIO2	VCCIO2	VCCIO2	–	VCCIO2
2	272	I/O	137	197	228	B9	C13	C7
2	273	I/O	–	–	–	–	D13	A6
2	274	I/O	–	196	227	–	B12	B7
2	275	I/O	136	195	226	E7	E13	C8
2	276	I/O	–	–	225	–	A12	A7

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	144-Pin TQFP (1)	208-Pin PQFP (1)	240-Pin PQFP (1)	144-Pin FineLine BGA	324-Pin FineLine BGA	356-Pin BGA
2	277	I/O	135	194	224	D7	C12	B8
–	278	GNDIO	GND	GND	GND	GND	GND	GND
2	279	I/O	–	193	223	–	D12	C9
2	280	I/O	133	192	222	C7	A11	A8
2	281	I/O	–	–	221	–	B11	B9
2	282	I/O	132	191	220	B8	A10	A9
2	283	I/O	–	–	–	–	D11	C10
2	284	I/O	–	190	219	–	A9	B10
–	285	VCCIO	VCCIO2	VCCIO2	VCCIO2	VCCIO2	VCCIO2	VCCIO2
2	286	I/O	–	–	–	–	G10	A10
2	287	I/O	131	188	217	C6	C11	C11
2	288	I/O	–	–	216	–	F11	B11
2	289	I/O	130	187	215	B7	E12	A11
–	290	TRST (6)	129	186	214	A10	B10	B12
–	291	NCEO	128	185	213	A9	C10	A12
1	292	FAST1	127	184	212	A8	D10	A13
–	293	GNDINT	GND	GND	GND	GND	GND	GND
–	294	GNDINT	–	–	–	–	–	–
–	295	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
–	296	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
–	297	GNDINT	GND	GND	GND	GND	GND	GND
–	298	VCCIO	VCCIO1	VCCIO1	VCCIO1	VCCIO1	VCCIO1	VCCIO1
1	299	FAST2	124	181	209	A5	B9	A15
–	300	TDO (6)	123	180	208	A4	C9	B15
–	301	GNDINT	–	–	–	–	GND	–
1	302	I/O	122	179	207	B6	D9	C15
1	303	I/O, INITDONE (4)	121	178	206	D6	E11	A16
1	304	I/O, RDYnBSY (2)	120	177	205	E6	E10	B16
1	305	I/O	–	–	–	–	B8	A17
1	306	I/O, CLKUSR (2)	119	176	204	F6	F10	C16
1	307	I/O	–	–	203	–	A8	B17
1	308	I/O	118	175	202	B5	A7	C17
1	309	I/O	–	174	201	–	E9	A18
1	310	I/O, DATA1 (2)	117	173	200	C5	F9	B18
1	311	I/O	–	–	–	–	D8	A19
–	312	GNDIO	GND	GND	GND	GND	GND	GND
–	313	VCCIO	VCCIO1	VCCIO1	VCCIO1	VCCIO1	–	VCCIO1
1	314	I/O	–	171	198	–	A6	C18
1	315	I/O	–	–	197	–	B7	B19
1	316	I/O	–	170	196	–	C8	A20
1	317	I/O, DATA2 (2)	115	168	195	D5	E8	B20
1	318	I/O	–	167	–	–	C7	C19
1	319	I/O	114	166	194	E5	A5	A21
1	320	I/O	–	165	193	–	B5	C20
1	321	I/O	113	164	192	B4	F8	B21
1	322	I/O	–	–	–	–	D7	A22

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	144-Pin TQFP (1)	208-Pin PQFP (1)	240-Pin PQFP (1)	144-Pin FineLine BGA	324-Pin FineLine BGA	356-Pin BGA
1	323	I/O	–	–	191	–	A4	C21
–	324	VCCIO	VCCIO1	VCCIO1	VCCIO1	VCCIO1	VCCIO1	VCCIO1
1	325	I/O	–	–	190	–	B4	A23
1	326	I/O, DATA3 (2)	112	163	189	C4	B6	B22
1	327	I/O	–	162	187	–	A3	B23
1	328	I/O	–	161	186	–	C6	C22
1	329	I/O	–	–	–	–	D6	A24
1	330	I/O, DATA4 (2)	111	160	185	C3	C5	A25
1	331	I/O	–	159	184	–	E7	B24
1	332	I/O	110	158	183	A3	B3	C23
1	333	I/O	–	–	182	–	A2	B25
1	334	I/O, DATA5 (2)	109	157	181	B3	B2	C24
–	335	GNDIO	GND	GND	GND	GND	GND	GND
–	336	–	–	–	–	–	–	–

Pin Name	144-Pin TQFP (1)	208-Pin PQFP (1)	240-Pin PQFP (1)	144-Pin FineLine BGA	324-Pin FineLine BGA	356-Pin FineLine BGA
MSEL0 (6)	18	25	29	F11	J17	P1
MSEL1 (6)	19	26	30	F10	J16	P2
NSTATUS (6)	57	82	92	M4	U9	AF15
NCONFIG (6)	22	29	33	G10	K17	R1
DCLK (6)	93	132	152	G2	J3	N25
CONF_DONE (6)	58	83	93	M3	U8	AE15
INIT_DONE (4)	121	178	206	D6	E11	A16
nCE (6)	91	130	150	H5	K2	P26
nCEO (6)	128	185	213	A9	C10	A12
nWS (2)	103	145	164	C2	K5	H22
nRS (2)	102	142	161	D2	J6	H24
nCS (2)	101	141	160	D3	H5	J24
CS (2)	98	138	157	E3	M2	K25
RDYnBSY (2)	120	177	205	E6	E10	B16
CLKUSR (2)	119	176	204	F6	F10	C16
DATA7 (2)	104	146	166	C1	H6	G23
DATA6 (2)	105	150	169	B2	G4	F24
DATA5 (2)	109	157	181	B3	B2	C24
DATA4 (2)	111	160	185	C3	C5	A25
DATA3 (2)	112	163	189	C4	B6	B22
DATA2 (2)	115	168	195	D5	E8	B20
DATA1 (2)	117	173	200	C5	F9	B18
DATA0 (6), (11)	94	133	153	G3	J2	M26
TDI (6)	90	129	149	H2	K3	P25
TDO (6)	123	180	208	A4	C9	B15
TCK (6)	52	76	87	M9	U10	AE12
TMS (6)	51	75	86	M10	U11	AF11
TRST (6)	129	186	214	A10	B10	B12
Dedicated Fast I/O Pins	53, 56, 124, 127	77, 81, 181, 184	88, 91, 209, 212	A8, A5, M8, M5	D10, B9, T10, T9	A13, A15, AF12, AE14
CLK1p	20	27	31	F9	K16	P3
CLK2p	92	131	151	G7	J4	N26
CLK3p	23	31	34	G8	H15	R4
CLK4p	95	134	154	F2	L2	M23
LOCK2 (9)	80	119	138	K3	N2	T24
LOCK4 (9)	78	116	135	L2	R3	V25
CLKLK_ENA (6), (10)	21	28	32	G9	K12	P4
CLKLK_OUT2p (8)	81	120	139	J2	M3	R23
CLKLK_FB2p	96	135	155	F4	N4	L25
DEV_CLRn (4)	97	137	156	E4	L5	L23
DEV_OE (4)	84	124	143	J3	L4	R26
VCCINT	1, 16, 36, 55, 73, 86, 108, 125	1, 23, 52, 79, 105, 126, 156, 182	1, 27, 60, 90, 122, 145, 179, 210	A7, B1, B12, F1, F12, H1, H12, M7	G6, G11, F7, H9, H12, J8, K11, L7, L10, M8, M13, N5, N12	A14, AB25, AB3, AF13, AF14, B14, E23, E1, H1, J23, L1, M25, R2, T22, U4, Y26

Pin Name	144-Pin TQFP (1)	208-Pin PQFP (1)	240-Pin PQFP (1)	144-Pin FineLine BGA	324-Pin FineLine BGA	356-Pin FineLine BGA
VCCIO1	116	172	199	A2	E6, G8	C14, A26
VCCIO2	144	208	229	A11	F12, H10	A1, C12
VCCIO3	5	8,189	12	D12	J11, G13	M5, C1
VCCIO4	45	80	67	K12	L12, N14	AD1, P5
VCCIO5	28	42,53	45	M11	M11, P13	AD12, AF1
VCCIO6	89	115	148	M2	L9, N7, P6	AF26, AD14
VCCIO7	61	86	97,120	K1	K8, M6	P22, AD26
VCCIO8	107	136	177	D1	F5, H7	C26, M22
VCC_CKLK2 (3)	85	125	144	G6	J7	P23
VCC_CKLK4 (3)	100	140	159	D4	K6	K24
VCC_CKOUT2 (7)	83	123	142	H4	P3	R25
GND	4, 12, 17, 34, 42, 54, 72, 74, 77, 87, 106, 126, 134	10, 16, 24, 39, 43, 64, 78, 95, 114, 118, 127, 143, 149, 169, 183, 199	19, 26, 28, 42, 56, 78, 89, 108, 132, 137, 146, 162, 165, 188, 211, 218, 240	A6, E1, E12, G1, G12, J1, J12, M6, A1, A12, M1, M12	D4, D15, E5, E14, F6, F13, G7, G9, G12, H8, H11, J9, J10, K9, K10, L8, L11, M7, M12, N6, N13, P5, P14, R4, R15	AB4, AB5, AC3, AC22, AC23, AC24, AD2, AD13, AD25, AE1, AE13, AE26, B1, B13, B26, C2, C13, C25, D3, D4, D22, D23, D24, E5, N3, N4, N5, N22, N23, N24
GND_CKLK2 (3)	88	128	147	G5	K7	P24
GND_CKLK4 (3)	99	139	158	E2	L6	L22
GND_CKOUT2 (7)	82	122	141	H3	P2	R24
No Connect (N.C.)	–	–	–	–	–	AA26, AA25, AA3, AA2, AA1, AA24, AA23, AB26, AB2, AB1, AB24, AB23, AB22, AC26, AC25, AC2, AC1, D2, D1, E4, E3, E2, J25, K26, K23
Total User I/O Pins (12)	92	151	183	93	246	246

Notes:

(1) For the 144-pin, 208-pin, and 240-pin PQFP packages, four unique VCCIO levels are supported. The VCCIO pins for I/O banks 1 and 8 must be at the same level; the VCCIO pins for banks 6 and 7 must be at the same level; the VCCIO pins for I/O banks 2 and 3 must be at the same level. However, unique VREF settings are supported for each of the eight I/O banks.

(2) This pin can be used as a user I/O pin after configuration.

(3) This pin is the power or ground for the ClockLock and ClockBoost circuitry. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device. VCC_CKLK has the same voltage specifications as the VCCINT and should be connected to a 1.8-V power supply. If the ClockLock or ClockBoost circuitry is not used, this power or ground pin should be connected to VCCINT or GNDINT, respectively.

(4) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.

(5) This pin is the complementary signal for the LVDS pair on dedicated inputs and outputs that can be configured for the LVDS standard. If not used for the LVDS pair, these pins are regular I/O pins. Pins with the "n" suffix carry the negative signal for the LVDS channel. Pins with a "p" suffix carry the positive signal for the LVDS channel.

(6) This pin is a dedicated pin; it is not available as a user I/O pin.

(7) This pin is the power or ground for the external output of a PLL. These pins should be set to the VCCIO level/standard desired for the external clock ouput. To ensure noise resistance, the power and ground supply to the PLL external output should be isolated from the power and ground to the rest of the VCCIO and GNDIO pins. If the PLL or external output is not used, this power or ground pin should be connected to VCCIO or GNDIO, respectively.

(8) The CLKLK_OUT pin is powered by the VCC_CKOUT and GND_CKOUT pins.

(9) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry is locked to the incoming clock and generates an internal clock, LOCK is driven high. LOCK remains high if a periodic clock stops clocking. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.

(10) This pin is the active high enable pin for all of the PLL circuits in the device. When de-asserted, all PLLs are reset to their default, unlocked state and will stop clocking. Once re-asserted, the PLLs will lock again and start clocking. If this pin function is not needed, the pin should be connected to VCCINT.

(11) This pin is tri-stated in user mode.

(12) The user I/O pin count includes dedicated inputs and dedicated clock inputs. It does not include the dedicated clock feedback and output pins.

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	1,020-Pin FineLine BGA
1	1	I/O	–	B28
1	2	I/O	–	C28
1	3	I/O	–	M20
–	4	VCCIO	VCCIO1	VCCIO1
1	5	I/O	–	P18
1	6	I/O	–	N18
1	7	I/O	–	N19
–	8	VCCINT	VCCINT	VCCINT
–	9	GNDINT	GND	GND
1	10	I/O	–	R17
1	11	I/O	–	N17
1	12	I/O	–	M18
1	13	I/O	–	M19
–	14	GNDIO	GND	GND
8	15	I/O	–	M17
8	16	I/O	F6	P17
8	17	I/O	–	M16
8	18	I/O	–	M15
–	19	VCCINT	VCCINT	VCCINT
–	20	GNDINT	GND	GND
8	21	I/O	–	R16
8	22	I/O	F5	M14
8	23	I/O	–	P16
8	24	I/O	F4	N16
–	25	VCCIO	VCCIO8	VCCIO8
8	26	I/O	–	P15
8	27	I/O	C1	N15
8	28	I/O	–	N14
8	29	I/O	D1	F6
–	30	VCCINT	VCCINT	VCCINT
–	31	GNDINT	GND	GND
8	32	I/O	–	M12
8	33	I/O	E2	R15
8	34	I/O	–	D5
8	35	I/O	G6	M13
–	36	GNDIO	GND	GND
8	37	I/O	–	N13
8	38	I/O	G5	P14
8	39	I/O	–	E6
8	40	I/O	G4	C5
–	41	VCCINT	VCCINT	VCCINT
–	42	GNDINT	GND	GND
8	43	I/O	–	E4
8	44	I/O	G3	G7
8	45	I/O	–	T16
8	46	I/O	F2	E5
–	47	VCCIO	VCCIO8	VCCIO8
8	48	I/O	–	H7

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	1,020-Pin FineLine BGA
8	49	I/O	E1	G6
8	50	I/O	–	F5
8	51	I/O	G2	G5
–	52	VCCINT	VCCINT	VCCINT
–	53	GNDINT	GND	GND
8	54	I/O	–	J8
8	55	I/O	H6	M11
8	56	I/O	–	H6
8	57	I/O	H4	N12
–	58	GNDIO	GND	GND
8	59	I/O	–	K8
8	60	I/O	H3	H5
8	61	I/O	–	J6
8	62	I/O	F1	J7
–	63	VCCINT	VCCINT	VCCINT
–	64	GNDINT	GND	GND
8	65	I/O	–	H4
8	66	I/O	H2	M10
8	67	I/O	–	K7
8	68	I/O	G1	J5
–	69	VCCIO	VCCIO8	VCCIO8
8	70	I/O	–	P13
8	71	I/O	–	–
8	72	I/O	J6	N11
8	73	I/O	–	M9
8	74	I/O	J5	K6
–	75	VCCINT	VCCINT	VCCINT
–	76	GNDINT	GND	GND
8	77	I/O	–	J4
8	78	I/O	–	R14
8	79	I/O	J4	L8
8	80	I/O	–	K5
8	81	I/O	J3	P12
–	82	GNDIO	GND	GND
8	83	I/O	–	L7
8	84	I/O	–	N10
8	85	I/O	J2	M8
8	86	I/O	–	L6
8	87	I/O	J1	M7
–	88	VCCINT	VCCINT	VCCINT
–	89	GNDINT	GND	GND
8	90	I/O	–	L5
8	91	I/O	–	K4
8	92	I/O	K6	N9
8	93	I/O	–	P11
8	94	I/O	K5	M6
–	95	VCCIO	VCCIO8	VCCIO8
8	96	I/O	–	N8

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	1,020-Pin FineLine BGA
8	97	I/O	–	P10
8	98	I/O	K4	M5
8	99	I/O	–	N7
8	100	I/O	K3	R13
–	101	VCCINT	VCCINT	VCCINT
–	102	GNDINT	GND	GND
8	103	I/O	–	R12
8	104	I/O	–	N6
8	105	I/O	K2	P8
8	106	I/O	–	N5
8	107	I/O	K1	N4
–	108	GNDIO	GND	GND
8	109	I/O	–	T15
8	110	I/O	–	P7
8	111	I/O, DATA6 (1)	L6	A4
8	112	I/O	L5	P6
8	113	I/O	L4	R11
–	114	VCCINT	VCCINT	VCCINT
–	115	GNDINT	GND	GND
8	116	I/O	L2	P4
8	117	I/O	L1	R10
8	118	I/O, DATA7 (1)	M6	B4
8	119	I/O	M5	T14
8	120	I/O	M4	P5
–	121	VCCIO	VCCIO8	VCCIO8
8	122	I/O	M3	R9
8	123	I/O	M2	R8
8	124	I/O, nWS (1)	M1	C4
8	125	I/O	N6	R7
8	126	I/O	N5	R6
–	127	VCCINT	VCCINT	VCCINT
–	128	GNDINT	GND	GND
8	129	I/O	N3	R4
8	130	I/O	N2	T13
8	131	I/O, nRS (1)	N1	D4
8	132	I/O	P6	R5
8	133	I/O	P5	T12
–	134	GNDIO	GND	GND
8	135	I/O	P4	T10
8	136	I/O	P3	T4
8	137	I/O, nCS (1)	P2	D3
8	138	I/O	P1	T8
8	139	I/O	R6	T11
–	140	VCCINT	VCCINT	VCCINT
–	141	GNDINT	GND	GND
–	142	VCC_CKLK4 (2)	R4	P9
–	143	GND_CKLK4 (2)	R3	T9
–	144	GND_CKLK4 (2)	R3	T9

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	1,020-Pin FineLine BGA
8	145	I/O, CS (1)	R2	E3
8	146	I/O	R1	T7
8	147	I/O, DEV_CLRn (3)	T6	H3
–	148	VCCIO	VCCIO8	VCCIO8
8	149	I/O, CLKLK_FB2n (4)	T5	J3
8	150	CLKLK_FB2p	T4	K3
8	151	I/O, CLK4n (4)	T3	N3
8	152	CLK4p	T2	P3
8	153	I/O, CLK2n (4)	T1	R3
–	154	VCCINT	VCCINT	VCCINT
–	155	GNDINT	GND	GND
–	156	VCCINT	VCCINT	VCCINT
–	157	GNDINT	GND	GND
–	158	DATA0 (5), (6)	U4	V3
–	159	DCLK (5)	U3	W3
8	160	CLK2p	U2	Y3
–	161	nCE (5)	U1	AC3
–	162	TDI (5)	W1	AD3
–	163	GND_CKLK2 (2)	W2	V9
–	164	GND_CKLK2 (2)	W2	V9
–	165	GNDINT	GND	GND
–	166	VCCINT	VCCINT	VCCINT
–	167	VCC_CKLK2 (2)	W4	Y9
–	168	GNDINT	GND	GND
–	169	VCCINT	VCCINT	VCCINT
–	170	VCCIO	VCCIO7	VCCIO7
7	171	I/O, DEV_OE (3)	Y5	AE3
–	172	VCC_CKOUT2 (7)	Y1	AA9
–	173	GND_CKOUT2 (7)	Y2	W9
–	174	CLKLK_OUT2p (8)	Y3	AH3
7	175	I/O, CLKLK_OUT2n (4)	Y4	AJ3
–	176	GNDIO	GND	GND
7	177	I/O, LVDSTXINCLK1p	W5	AM5
7	178	I/O, LVDSTXINCLK1n (4)	Y6	AL5
7	179	I/O, LOCK2 (9)	AB6	AK4
7	180	I/O, LVDSTXOUTCLK1n	AA2	AM4
7	181	I/O, LVDSTXOUTCLK1p	AA3	AL4
–	182	GNDINT	GND	GND
–	183	VCCINT	VCCINT	VCCINT
7	184	I/O, LVDSTX01p	AA5	D1
7	185	I/O, LVDSTX01n (4)	AA6	D2
7	186	I/O	AA1	T6
7	187	I/O, LVDSTX02n (4)	AB2	E1
7	188	I/O, LVDSTX02p	AB3	E2
–	189	VCCIO	VCCIO7	VCCIO7
7	190	I/O, LVDSTX03p	AB4	H1

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	1,020-Pin FineLine BGA
7	191	I/O, LVDSTX03n (4)	AB5	H2
7	192	I/O	AB1	T5
7	193	I/O, LVDSTX04n (4)	AC1	J1
7	194	I/O, LVDSTX04p	AC2	J2
–	195	GNDINT	GND	GND
–	196	VCCINT	VCCINT	VCCINT
7	197	I/O, LVDSTX05p	AC4	K1
7	198	I/O, LVDSTX05n (4)	AC5	K2
7	199	I/O, LOCK4 (9)	AC6	AK5
7	200	I/O, LVDSTX06n (4)	AD1	N1
7	201	I/O, LVDSTX06p	AD2	N2
–	202	GNDIO	GND	GND
7	203	I/O, LVDSTX07p	AD3	P1
7	204	I/O, LVDSTX07n (4)	AD4	P2
7	205	I/O	AD5	U4
7	206	I/O, LVDSTX08n (4)	AD6	R1
7	207	I/O, LVDSTX08p	AE1	R2
–	208	GNDINT	GND	GND
–	209	VCCINT	VCCINT	VCCINT
7	210	I/O, LVDSTX09p	AE3	V1
7	211	I/O, LVDSTX09n (4)	AE4	V2
7	212	I/O	AE5	U6
7	213	I/O, LVDSTX10n (4)	AE6	W1
7	214	I/O, LVDSTX10p	AF1	W2
–	215	VCCIO	VCCIO7	VCCIO7
7	216	I/O, LVDSTX11p	AF2	Y1
7	217	I/O, LVDSTX11n (4)	AF3	Y2
7	218	I/O	AF4	U5
7	219	I/O, LVDSTX12n (4)	AF5	AC1
7	220	I/O, LVDSTX12p	AF6	AC2
–	221	GNDINT	GND	GND
–	222	VCCINT	VCCINT	VCCINT
7	223	I/O, LVDSTX13p	AH1	AD1
7	224	I/O, LVDSTX13n (4)	AG2	AD2
7	225	I/O	AG3	U8
7	226	I/O, LVDSTX14n (4)	AG4	AE1
7	227	I/O, LVDSTX14p	AG5	AE2
–	228	GNDIO	GND	GND
7	229	I/O, LVDSTX15p	AG6	AH1
7	230	I/O, LVDSTX15n (4)	AJ1	AH2
7	231	I/O	AH2	U7
7	232	I/O, LVDSTX16n (4)	AK1	AJ1
7	233	I/O, LVDSTX16p	AH3	AJ2
–	234	GNDINT	GND	GND
–	235	VCCINT	VCCINT	VCCINT
7	236	I/O	AH5	U9
7	237	I/O	–	V6
7	238	I/O	AH6	V4

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	1,020-Pin FineLine BGA
7	239	I/O	–	U11
7	240	I/O	–	U10
–	241	VCCIO	VCCIO7	VCCIO7
7	242	I/O	–	V8
7	243	I/O	–	U13
7	244	I/O	AJ2	V5
7	245	I/O	–	U12
7	246	I/O	–	W4
–	247	GNDINT	GND	GND
–	248	VCCINT	VCCINT	VCCINT
7	249	I/O	–	V7
7	250	I/O	–	–
7	251	I/O	AL1	W6
7	252	I/O	–	–
7	253	I/O	–	U14
–	254	GNDIO	GND	GND
7	255	I/O	–	W8
7	256	I/O	–	W7
7	257	I/O	AK2	V10
7	258	I/O	–	W5
–	259	GNDINT	GND	GND
–	260	VCCINT	VCCINT	VCCINT
7	261	I/O	–	Y4
7	262	I/O	–	V11
7	263	I/O	AJ3	V12
7	264	I/O	–	Y5
–	265	VCCIO	VCCIO7	VCCIO7
7	266	I/O	–	Y7
7	267	I/O	–	W10
7	268	I/O	AJ4	U15
7	269	I/O	–	Y6
–	270	GNDINT	GND	GND
–	271	VCCINT	VCCINT	VCCINT
7	272	I/O	–	Y8
7	273	I/O	–	V13
7	274	I/O	AJ5	AA6
7	275	I/O	–	AA5
–	276	GNDIO	GND	GND
7	277	I/O	–	AB5
7	278	I/O	–	AA8
7	279	I/O	AJ6	AA7
7	280	I/O	–	W11
–	281	GNDINT	GND	GND
–	282	VCCINT	VCCINT	VCCINT
7	283	I/O	–	V14
7	284	I/O	–	AC5
7	285	I/O	AM1	Y10
7	286	I/O	–	AC4

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	1,020-Pin FineLine BGA
–	287	VCCIO	VCCIO7	VCCIO7
7	288	I/O	–	Y11
7	289	I/O	–	AB7
7	290	I/O	AK3	AB6
7	291	I/O	–	W12
–	292	GNDINT	GND	GND
–	293	VCCINT	VCCINT	VCCINT
7	294	I/O	–	AD4
7	295	I/O	–	AC6
7	296	I/O	AK4	AC7
7	297	I/O	–	AE4
–	298	GNDIO	GND	GND
7	299	I/O	–	Y12
7	300	I/O	–	W13
7	301	I/O	AK5	AD5
7	302	I/O	–	AA10
–	303	GNDINT	GND	GND
–	304	VCCINT	VCCINT	VCCINT
7	305	I/O	–	AD6
7	306	I/O	–	AE5
7	307	I/O	AK6	AE6
7	308	I/O	–	AD7
–	309	VCCIO	VCCIO7	VCCIO7
–	310	VCCIO	VCCIO6	VCCIO6
6	311	I/O	–	AA11
6	312	I/O	–	AE7
6	313	I/O	–	AH4
6	314	I/O	–	AF5
–	315	GNDINT	GND	GND
–	316	VCCINT	VCCINT	VCCINT
6	317	I/O	–	AF6
6	318	I/O	–	AG5
6	319	I/O	–	AG6
–	320	GNDIO	GND	GND
6	321	I/O	–	AA12
6	322	I/O	–	W14
6	323	I/O	–	U16
6	324	I/O	AL7	AJ4
6	325	I/O	–	AJ5
6	326	I/O	AM6	AH6
6	327	I/O	–	AF7
6	328	I/O	AP3	AG7
–	329	VCCIO	VCCIO6	VCCIO6
6	330	I/O	AN5	AH7
6	331	I/O	AR2	AB8
6	332	I/O	AP4	AC8
6	333	I/O	AL8	AD8
6	334	I/O	AM7	AE8

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	1,020-Pin FineLine BGA
6	335	I/O	–	AF8
6	336	I/O	AN6	AG8
6	337	I/O	–	AH8
6	338	I/O	AR3	AJ8
6	339	I/O	–	AK8
–	340	GNDIO	GND	GND
6	341	I/O	–	AL8
6	342	I/O	AP5	AM8
6	343	I/O	–	AB9
6	344	I/O	AL9	AC9
6	345	I/O	–	AD9
6	346	I/O	AR4	AE9
6	347	I/O	AM8	AF9
6	348	I/O	AN7	AG9
6	349	I/O	AP6	AH9
6	350	I/O	AR5	AJ9
–	351	VCCIO	VCCIO6	VCCIO6
6	352	I/O	AM9	AK9
6	353	I/O	–	AL9
6	354	I/O	AL10	AM9
6	355	I/O	–	AB10
6	356	I/O	AN8	AC10
6	357	I/O	–	AD10
6	358	I/O	–	AE10
6	359	I/O	AP7	AF10
6	360	I/O	–	AG10
6	361	I/O	AR6	AH10
–	362	GNDIO	GND	GND
6	363	I/O	–	AJ10
6	364	I/O	AM10	AK10
6	365	I/O	AN9	AL10
6	366	I/O	AL11	AB11
6	367	I/O	AP8	AC11
6	368	I/O	AR7	AD11
6	369	I/O	AM11	AE11
6	370	I/O	–	AF11
6	371	I/O	AN10	AG11
6	372	I/O	–	–
6	373	I/O	AP9	AH11
–	374	VCCIO	VCCIO6	VCCIO6
–	375	VCCINT	VCCINT	VCCINT
–	376	VCCINT	VCCINT	VCCINT
–	377	GNDINT	GND	GND
–	378	GNDINT	GND	GND
6	379	I/O	AR8	AB12
6	380	I/O	–	–
6	381	I/O	AN11	AC12
6	382	I/O	–	AD12

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	1,020-Pin FineLine BGA
6	383	I/O	AP10	AE12
6	384	I/O	AR9	AF12
6	385	I/O	AL13	AG12
6	386	I/O	AM13	AH12
6	387	I/O	AN12	AB13
6	388	I/O	AP11	AC13
6	389	I/O	–	AD13
–	390	GNDIO	GND	GND
6	391	I/O	AL14	AE13
6	392	I/O	–	AF13
6	393	I/O	AR10	AG13
6	394	I/O	–	AH13
6	395	I/O	–	AJ13
6	396	I/O	AN13	AK13
6	397	I/O	–	AL13
6	398	I/O	AP12	AB14
6	399	I/O	–	AC14
6	400	I/O	AM14	AD14
–	401	VCCIO	VCCIO6	VCCIO6
6	402	I/O	AR11	AE14
6	403	I/O	AL15	AF14
6	404	I/O	AN14	AG14
6	405	I/O	AP13	AH14
6	406	I/O	AR12	AJ14
6	407	I/O	–	AK14
6	408	I/O	AR13	AL14
6	409	I/O	–	AB15
6	410	I/O	AM15	AC15
6	411	I/O	–	AD15
–	412	GNDIO	GND	GND
6	413	I/O	–	AE15
6	414	I/O	AN15	AF15
6	415	I/O	–	AG15
6	416	I/O	AL16	AH15
6	417	I/O	–	AJ15
6	418	I/O	AP14	AK15
6	419	I/O	AR14	AL15
6	420	I/O	AP15	AB16
6	421	I/O	AR15	AC16
6	422	I/O, LVDSDESKEW	AM16	AM10
–	423	VCCIO	VCCIO6	VCCIO6
6	424	I/O	AN16	AD16
6	425	I/O	–	AE16
6	426	I/O	AP16	AF16
6	427	I/O	–	AG16
6	428	I/O	AR16	AH16
–	429	CONF_DONE (5)	AM17	AM13
–	430	nSTATUS (5)	AN17	AM14

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	1,020-Pin FineLine BGA
5	431	FAST4	AP17	AM15
–	432	VCCINT	VCCINT	VCCINT
–	433	VCCINT	VCCINT	VCCINT
–	434	GNDINT	GND	GND
–	435	GNDINT	GND	GND
–	436	GNDIO	GND	GND
5	437	FAST3	AP19	AM18
–	438	TCK (5)	AN19	AM19
–	439	TMS (5)	AM19	AM20
5	440	I/O	AR20	AJ16
5	441	I/O	–	AK16
5	442	I/O	AP20	AK17
5	443	I/O	–	AJ17
5	444	I/O	AN20	AH17
–	445	VCCIO	VCCIO5	VCCIO5
5	446	I/O	AM20	AG17
5	447	I/O	AR21	AF17
5	448	I/O	AP21	AE17
5	449	I/O	AR22	AD17
5	450	I/O	AP22	AC17
5	451	I/O	–	AB17
5	452	I/O	AL20	AL18
5	453	I/O	–	AK18
5	454	I/O	AN21	AJ18
5	455	I/O	–	AH18
–	456	GNDIO	GND	GND
5	457	I/O	–	AG18
5	458	I/O	AM21	AF18
5	459	I/O	–	AE18
5	460	I/O	AR23	AD18
5	461	I/O	–	AC18
5	462	I/O	AR24	AB18
5	463	I/O	AP23	AL19
5	464	I/O	AN22	AK19
5	465	I/O	AL21	AJ19
5	466	I/O	AR25	AH19
–	467	VCCIO	VCCIO5	VCCIO5
5	468	I/O	AM22	AG19
5	469	I/O	–	AF19
5	470	I/O	AP24	AE19
5	471	I/O	–	AD19
5	472	I/O	AN23	AC19
5	473	I/O	–	AB19
5	474	I/O	–	AL20
5	475	I/O	AR26	AK20
5	476	I/O	–	AJ20
5	477	I/O	AL22	AH20
–	478	GNDIO	GND	GND

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	1,020-Pin FineLine BGA
5	479	I/O	–	AG20
5	480	I/O	AP25	AF20
5	481	I/O	AN24	AE20
5	482	I/O	AM23	AD20
5	483	I/O	AL23	AC20
5	484	I/O	AR27	AB20
5	485	I/O	AP26	AH21
5	486	I/O	–	AG21
5	487	I/O	AN25	AF21
5	488	I/O	–	–
5	489	I/O	AR28	AE21
–	490	VCCIO	VCCIO5	VCCIO5
–	491	VCCINT	VCCINT	VCCINT
–	492	VCCINT	VCCINT	VCCINT
–	493	GNDINT	GND	GND
–	494	GNDINT	GND	GND
5	495	I/O	AP27	AD21
5	496	I/O	–	–
5	497	I/O	AN26	AC21
5	498	I/O	–	AB21
5	499	I/O	AM25	AH22
5	500	I/O	AR29	AG22
5	501	I/O	AP28	AF22
5	502	I/O	AL25	AE22
5	503	I/O	AN27	AD22
5	504	I/O	AM26	AC22
5	505	I/O	–	AB22
–	506	GNDIO	GND	GND
5	507	I/O	AR30	AM23
5	508	I/O	–	AL23
5	509	I/O	AP29	AK23
5	510	I/O	–	AJ23
5	511	I/O	–	AH23
5	512	I/O	AN28	AG23
5	513	I/O	–	AF23
5	514	I/O	AL26	AE23
5	515	I/O	–	AD23
5	516	I/O	AM27	AC23
–	517	VCCIO	VCCIO5	VCCIO5
5	518	I/O	AR31	AB23
5	519	I/O	AP30	AM24
5	520	I/O	AN29	AL24
5	521	I/O	AM28	AK24
5	522	I/O	AR32	AJ24
5	523	I/O	–	AH24
5	524	I/O	AL27	AG24
5	525	I/O	–	AF24
5	526	I/O	AP31	AE24

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	1,020-Pin FineLine BGA
5	527	I/O	–	AD24
–	528	GNDIO	GND	GND
5	529	I/O	–	AC24
5	530	I/O	AR33	AB24
5	531	I/O	–	AM25
5	532	I/O	AN30	AL25
5	533	I/O	–	AK25
5	534	I/O	AM29	AJ25
5	535	I/O	AL28	AH25
5	536	I/O	AP32	AG25
5	537	I/O	AR34	AF25
5	538	I/O	AN31	AE25
–	539	VCCIO	VCCIO5	VCCIO5
5	540	I/O	AP33	AD25
5	541	I/O	–	AC25
5	542	I/O	AM30	AB25
5	543	I/O	–	AH26
5	544	I/O	AL29	AG26
5	545	I/O	–	V15
5	546	I/O	–	Y13
5	547	I/O	–	AH5
–	548	GNDIO	GND	GND
5	549	I/O	–	AA13
5	550	I/O	–	Y14
5	551	I/O	–	AA14
–	552	VCCINT	VCCINT	VCCINT
–	553	GNDINT	GND	GND
5	554	I/O	–	AA15
5	555	I/O	–	W15
5	556	I/O	–	Y15
5	557	I/O	–	V16
–	558	VCCIO	VCCIO5	VCCIO5
–	559	VCCIO	VCCIO4	VCCIO4
4	560	I/O	–	Y16
4	561	I/O	AL33	W16
4	562	I/O	–	AA17
4	563	I/O	AK30	W17
–	564	VCCINT	VCCINT	VCCINT
–	565	GNDINT	GND	GND
4	566	I/O	–	AA18
4	567	I/O	AK31	Y18
4	568	I/O	–	Y17
4	569	I/O	AK32	AA16
–	570	GNDIO	GND	GND
4	571	I/O	–	AA19
4	572	I/O	AL34	V17
4	573	I/O	–	AA20
4	574	I/O	AM35	AH27

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	1,020-Pin FineLine BGA
–	575	VCCINT	VCCINT	VCCINT
–	576	GNDINT	GND	GND
4	577	I/O	–	AK29
4	578	I/O	AJ30	AA21
4	579	I/O	–	AK28
4	580	I/O	AJ31	W18
–	581	VCCIO	VCCIO4	VCCIO4
4	582	I/O	–	W19
4	583	I/O	AJ32	AJ29
4	584	I/O	–	AJ28
4	585	I/O	AJ33	Y19
–	586	VCCINT	VCCINT	VCCINT
–	587	GNDINT	GND	GND
4	588	I/O	–	Y20
4	589	I/O	AK34	U17
4	590	I/O	–	AG27
4	591	I/O	AL35	V18
–	592	GNDIO	GND	GND
4	593	I/O	–	AG28
4	594	I/O	AJ34	AH28
4	595	I/O	–	AF26
4	596	I/O	AH30	AH29
–	597	VCCINT	VCCINT	VCCINT
–	598	GNDINT	GND	GND
4	599	I/O	–	AF28
4	600	I/O	AH32	AE26
4	601	I/O	–	AF27
4	602	I/O	AH33	AJ30
–	603	VCCIO	VCCIO4	VCCIO4
4	604	I/O	–	AH30
4	605	I/O	AK35	AA22
4	606	I/O	–	AD26
4	607	I/O	AH34	AE28
–	608	VCCINT	VCCINT	VCCINT
–	609	GNDINT	GND	GND
4	610	I/O	AJ35	AA23
4	611	I/O	AG30	AD27
4	612	I/O	–	Y21
4	613	I/O	AG31	AE27
–	614	GNDIO	GND	GND
4	615	I/O	AG32	AE29
4	616	I/O	–	–
4	617	I/O	AG33	W20
4	618	I/O	–	AC26
4	619	I/O	AG34	AE30
–	620	VCCINT	VCCINT	VCCINT
–	621	GNDINT	GND	GND
4	622	I/O	AG35	AD28

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	1,020-Pin FineLine BGA
4	623	I/O	–	AD29
4	624	I/O	AF30	AA24
4	625	I/O	–	V19
4	626	I/O	AF31	Y22
–	627	VCCIO	VCCIO4	VCCIO4
4	628	I/O	AF32	W21
4	629	I/O	–	AC28
4	630	I/O	AF33	AB26
4	631	I/O	–	AC27
4	632	I/O	AF34	AD30
–	633	VCCINT	VCCINT	VCCINT
–	634	GNDINT	GND	GND
4	635	I/O	AF35	AC29
4	636	I/O	–	AB28
4	637	I/O	AE30	AA25
4	638	I/O	–	Y23
4	639	I/O	AE31	AB27
–	640	GNDIO	GND	GND
4	641	I/O	AE32	W22
4	642	I/O	–	Y24
4	643	I/O	AE34	AA26
4	644	I/O	–	AA27
4	645	I/O	AE35	W23
–	646	VCCINT	VCCINT	VCCINT
–	647	GNDINT	GND	GND
4	648	I/O	AD30	V20
4	649	I/O	–	V21
4	650	I/O	AD31	Y26
4	651	I/O	–	AA28
4	652	I/O	AD32	Y25
–	653	VCCIO	VCCIO4	VCCIO4
4	654	I/O	AD33	W25
4	655	I/O	–	Y27
4	656	I/O	AD34	U18
4	657	I/O	–	Y28
4	658	I/O	AD35	V22
–	659	VCCINT	VCCINT	VCCINT
–	660	GNDINT	GND	GND
4	661	I/O	AC30	Y29
4	662	I/O	–	W29
4	663	I/O	AC31	V23
4	664	I/O	–	W27
4	665	I/O	AC33	W26
–	666	GNDIO	GND	GND
4	667	I/O	AC34	V25
4	668	I/O	–	W28
4	669	I/O	AC35	U19
4	670	I/O	–	V26

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	1,020-Pin FineLine BGA
4	671	I/O	AB30	U20
–	672	VCCINT	VCCINT	VCCINT
–	673	GNDINT	GND	GND
4	674	I/O	AB31	V27
4	675	I/O	–	U22
4	676	I/O	AB32	U21
4	677	I/O	–	V28
4	678	I/O	AB33	V29
–	679	VCCIO	VCCIO4	VCCIO4
4	680	I/O	AB34	U24
4	681	I/O	–	U29
4	682	I/O	AB35	U23
4	683	I/O	–	U25
4	684	I/O, LOCK1 (9)	AA30	AC30
–	685	VCCINT	VCCINT	VCCINT
–	686	GNDINT	GND	GND
4	687	I/O	AA32	U26
4	688	I/O	AA33	U27
4	689	I/O	AA34	U28
–	690	VCC_CKLK1 (2)	AA35	W24
–	691	GND_CKLK1 (2)	Y30	V24
–	692	GND_CKLK1 (2)	Y30	V24
–	693	GNDIO	GND	GND
4	694	I/O, CLKLK_FB1n (4)	Y31	AM28
4	695	CLKLK_FB1p	Y32	AL28
4	696	I/O, CLK3n (4)	Y33	Y30
4	697	CLK3p	Y34	W30
4	698	I/O, CLK1n (4)	Y35	V30
–	699	VCCIO	VCCIO4	VCCIO4
–	700	VCCINT	VCCINT	VCCINT
–	701	GNDINT	GND	GND
–	702	VCCINT	VCCINT	VCCINT
–	703	GNDINT	GND	GND
–	704	nCONFIG (5)	W32	R30
–	705	CLKLK_ENA (5), (10)	W33	P30
4	706	CLK1p	W34	N30
–	707	MSEL1 (5)	W35	K30
–	708	MSEL0 (5)	U35	J30
–	709	GNDINT	GND	GND
–	710	VCCINT	VCCINT	VCCINT
–	711	GNDINT	GND	GND
–	712	VCCINT	VCCINT	VCCINT
–	713	VCC_CKOUT1 (7)	U33	N24
–	714	GND_CKOUT1 (7)	U32	T24
–	715	CLKLK_OUT1p (8)	U31	AM29
3	716	I/O, CLKLK_OUT1n (4)	T35	AL29
–	717	VCC_CKLK3 (2)	T34	M24
–	718	VCCIO	VCCIO3	VCCIO3

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	1,020-Pin FineLine BGA
–	719	GND_CKLK3 (2)	V35	P23
–	720	GND_CKLK3 (2)	T33	P24
3	721	I/O, LVDSRXINCLK1p	T32	B29
3	722	I/O, LVDSRXINCLK1n (4)	T31	A29
3	723	I/O	T30	T27
3	724	I/O	R35	T29
–	725	GNDINT	GND	GND
–	726	VCCINT	VCCINT	VCCINT
3	727	I/O, LVDSRX01p	R33	AJ32
3	728	I/O, LVDSRX01n (4)	R32	AJ31
3	729	I/O, LOCK3 (9)	R31	H30
3	730	I/O, LVDSRX02n (4)	R30	AH32
3	731	I/O, LVDSRX02p	P35	AH31
–	732	GNDIO	GND	GND
3	733	I/O, LVDSRX03p	P34	AE32
3	734	I/O, LVDSRX03n (4)	P33	AE31
3	735	I/O	P32	T28
3	736	I/O, LVDSRX04n (4)	P31	AD32
3	737	I/O, LVDSRX04p	P30	AD31
–	738	GNDINT	GND	GND
–	739	VCCINT	VCCINT	VCCINT
3	740	I/O, LVDSRX05p	N34	AC32
3	741	I/O, LVDSRX05n (4)	N33	AC31
3	742	I/O	N32	T25
3	743	I/O, LVDSRX06n (4)	N31	Y32
3	744	I/O, LVDSRX06p	N30	Y31
–	745	VCCIO	VCCIO3	VCCIO3
3	746	I/O, LVDSRX07p	M35	W32
3	747	I/O, LVDSRX07n (4)	M34	W31
3	748	I/O	M33	T26
3	749	I/O, LVDSRX08n (4)	M32	V32
3	750	I/O, LVDSRX08p	M31	V31
–	751	GNDINT	GND	GND
–	752	VCCINT	VCCINT	VCCINT
3	753	I/O, LVDSRX09p	L35	R32
3	754	I/O, LVDSRX09n (4)	L34	R31
3	755	I/O	L33	T23
3	756	I/O, LVDSRX10n (4)	L32	P32
3	757	I/O, LVDSRX10p	L31	P31
–	758	GNDIO	GND	GND
3	759	I/O, LVDSRX11p	L30	N32
3	760	I/O, LVDSRX11n (4)	K35	N31
3	761	I/O	K34	T22
3	762	I/O, LVDSRX12n (4)	K33	K32
3	763	I/O, LVDSRX12p	K32	K31
–	764	GNDINT	GND	GND
–	765	VCCINT	VCCINT	VCCINT

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	1,020-Pin FineLine BGA
3	766	I/O, LVDSRX13p	K30	J32
3	767	I/O, LVDSRX13n (4)	J35	J31
3	768	I/O	H35	T21
3	769	I/O, LVDSRX14n (4)	J34	H32
3	770	I/O, LVDSRX14p	J33	H31
–	771	VCCIO	VCCIO3	VCCIO3
3	772	I/O, LVDSRX15p	J32	E32
3	773	I/O, LVDSRX15n (4)	J31	E31
3	774	I/O	J30	R29
3	775	I/O, LVDSRX16n (4)	G35	D32
3	776	I/O, LVDSRX16p	H34	D31
–	777	GNDINT	GND	GND
–	778	VCCINT	VCCINT	VCCINT
3	779	I/O	H33	R28
3	780	I/O	–	R27
3	781	I/O	H32	T20
3	782	I/O	–	R26
3	783	I/O	–	T19
–	784	GNDIO	GND	GND
3	785	I/O	–	R25
3	786	I/O	–	P29
3	787	I/O	H31	P26
3	788	I/O	–	P27
3	789	I/O	–	R24
–	790	GNDINT	GND	GND
–	791	VCCINT	VCCINT	VCCINT
3	792	I/O	–	R23
3	793	I/O	–	P28
3	794	I/O	H30	N29
3	795	I/O	–	P25
3	796	I/O	–	N26
–	797	VCCIO	VCCIO3	VCCIO3
3	798	I/O	–	R22
3	799	I/O	–	N27
3	800	I/O	G34	R21
3	801	I/O	–	N28
–	802	GNDINT	GND	GND
–	803	VCCINT	VCCINT	VCCINT
3	804	I/O	–	R20
3	805	I/O	–	T18
3	806	I/O	E35	M28
3	807	I/O	–	N25
–	808	GNDIO	GND	GND
3	809	I/O	–	M27
3	810	I/O	–	P22
3	811	I/O	F34	L28
3	812	I/O	–	K29
–	813	GNDINT	GND	GND

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	1,020-Pin FineLine BGA
–	814	VCCINT	VCCINT	VCCINT
3	815	I/O	–	M26
3	816	I/O	–	N23
3	817	I/O	G33	M25
3	818	I/O	–	L27
–	819	VCCIO	VCCIO3	VCCIO3
3	820	I/O	–	J29
3	821	I/O	–	R19
3	822	I/O	G32	K28
3	823	I/O	–	P21
–	824	GNDINT	GND	GND
–	825	VCCINT	VCCINT	VCCINT
3	826	I/O	–	J27
3	827	I/O	–	K26
3	828	I/O	G31	N22
3	829	I/O	–	L26
–	830	GNDIO	GND	GND
3	831	I/O	–	P20
3	832	I/O	–	M23
3	833	I/O	D35	K27
3	834	I/O	–	H29
–	835	GNDINT	GND	GND
–	836	VCCINT	VCCINT	VCCINT
3	837	I/O	–	J28
3	838	I/O	–	H28
3	839	I/O	E34	H27
3	840	I/O	–	N21
–	841	VCCIO	VCCIO3	VCCIO3
3	842	I/O	–	H26
3	843	I/O	–	E30
3	844	I/O	F33	J26
3	845	I/O	–	M22
–	846	GNDINT	GND	GND
–	847	VCCINT	VCCINT	VCCINT
3	848	I/O	–	G28
3	849	I/O	–	G27
3	850	I/O	F32	D30
3	851	I/O	–	E29
–	852	GNDIO	GND	GND
2	853	I/O	–	T17
2	854	I/O	–	M21
2	855	I/O	–	F28
2	856	I/O	–	D29
–	857	GNDINT	GND	GND
–	858	VCCINT	VCCINT	VCCINT
2	859	I/O	–	N20
2	860	I/O	–	P19
2	861	I/O	–	R18

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	1,020-Pin FineLine BGA
–	862	VCCIO	VCCIO2	VCCIO2
2	863	I/O	–	E28
2	864	I/O	–	D28
2	865	I/O	–	C29
2	866	I/O	E29	A28
2	867	I/O	–	F27
2	868	I/O	D30	E27
2	869	I/O	–	G26
2	870	I/O	B33	F26
–	871	GNDIO	GND	GND
2	872	I/O	C31	E26
2	873	I/O	A34	L25
2	874	I/O	B32	K25
2	875	I/O	E28	J25
2	876	I/O	D29	H25
2	877	I/O	–	G25
2	878	I/O	C30	F25
2	879	I/O	–	E25
2	880	I/O	A33	D25
2	881	I/O	–	C25
–	882	VCCIO	VCCIO2	VCCIO2
2	883	I/O	–	B25
2	884	I/O	B31	A25
2	885	I/O	–	L24
2	886	I/O	E27	K24
2	887	I/O	–	J24
2	888	I/O	A32	H24
2	889	I/O	D28	G24
2	890	I/O	C29	F24
2	891	I/O	B30	E24
2	892	I/O	A31	D24
–	893	GNDIO	GND	GND
2	894	I/O	D27	C24
2	895	I/O	–	B24
2	896	I/O	E26	L23
2	897	I/O	–	K23
2	898	I/O	C28	J23
2	899	I/O	–	H23
2	900	I/O	–	G23
2	901	I/O	B29	F23
2	902	I/O	–	E23
2	903	I/O	A30	D23
–	904	VCCIO	VCCIO2	VCCIO2
2	905	I/O	–	C23
2	906	I/O	D26	B23
2	907	I/O	C27	L22
2	908	I/O	E25	K22
2	909	I/O	B28	J22

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	1,020-Pin FineLine BGA
2	910	I/O	A29	H22
2	911	I/O	D25	G22
2	912	I/O	–	F22
2	913	I/O	C26	E22
2	914	I/O	–	–
2	915	I/O	B27	L21
–	916	GNDIO	GND	GND
–	917	GNDINT	GND	GND
–	918	GNDINT	GND	GND
–	919	VCCINT	VCCINT	VCCINT
–	920	VCCINT	VCCINT	VCCINT
–	921	GNDINT	–	–
2	922	I/O	A28	K21
2	923	I/O	–	–
2	924	I/O	C25	J21
2	925	I/O	–	H21
2	926	I/O	B26	G21
2	927	I/O	A27	F21
2	928	I/O	E23	E21
2	929	I/O	D23	L20
2	930	I/O	C24	K20
2	931	I/O	B25	J20
2	932	I/O	–	H20
–	933	VCCIO	VCCIO2	VCCIO2
2	934	I/O	E22	G20
2	935	I/O	–	F20
2	936	I/O	A26	E20
2	937	I/O	–	D20
2	938	I/O	–	C20
2	939	I/O	C23	B20
2	940	I/O	–	L19
2	941	I/O	B24	K19
2	942	I/O	–	J19
2	943	I/O	D22	H19
–	944	GNDIO	GND	GND
2	945	I/O	A25	G19
2	946	I/O	E21	F19
2	947	I/O	C22	E19
2	948	I/O	B23	D19
2	949	I/O	A24	C19
2	950	I/O	–	B19
2	951	I/O	A23	L18
2	952	I/O	–	K18
2	953	I/O	D21	J18
2	954	I/O	–	H18
–	955	VCCIO	VCCIO2	VCCIO2
2	956	I/O	–	G18
2	957	I/O	C21	F18

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	1,020-Pin FineLine BGA
2	958	I/O	–	E18
2	959	I/O	E20	D18
2	960	I/O	–	C18
2	961	I/O	B22	B18
2	962	I/O	A22	L17
2	963	I/O	B21	K17
2	964	I/O	A21	J17
2	965	I/O	D20	H17
–	966	GNDIO	GND	GND
2	967	I/O	C20	G17
2	968	I/O	–	F17
2	969	I/O	B20	E17
2	970	I/O	–	D17
2	971	I/O	A20	C17
–	972	VCCIO	VCCIO2	VCCIO2
–	973	TRST (5)	D19	A24
–	974	NCEO (5)	C19	A23
1	975	FAST1	B19	A20
–	976	GNDINT	GND	GND
–	977	GNDINT	GND	GND
–	978	VCCINT	VCCINT	VCCINT
–	979	VCCINT	VCCINT	VCCINT
–	980	VCCIO	VCCIO1	VCCIO1
1	981	FAST2	B17	A19
–	982	TDO (5)	C17	A18
–	983	GNDINT	GND	GND
1	984	I/O	A16	C16
1	985	I/O	–	D16
1	986	I/O	B16	E16
1	987	I/O	–	F16
1	988	I/O, INITDONE (3)	C16	A15
–	989	GNDIO	GND	GND
1	990	I/O	D16	G16
1	991	I/O	A15	H16
1	992	I/O	B15	J16
1	993	I/O, RDYnBSY (1)	A14	A14
1	994	I/O	B14	K16
1	995	I/O	–	L16
1	996	I/O	E16	B15
1	997	I/O	–	C15
1	998	I/O, CLKUSR (1)	C15	A13
1	999	I/O	–	D15
–	1000	VCCIO	VCCIO1	VCCIO1
1	1001	I/O	–	E15
1	1002	I/O	D15	F15
1	1003	I/O	–	G15
1	1004	I/O	A13	H15
1	1005	I/O	–	J15

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	1,020-Pin FineLine BGA
1	1006	I/O	A12	K15
1	1007	I/O	B13	L15
1	1008	I/O	C14	B14
1	1009	I/O	E15	C14
1	1010	I/O	A11	D14
–	1011	GNDIO	GND	GND
1	1012	I/O	D14	E14
1	1013	I/O	–	F14
1	1014	I/O	B12	G14
1	1015	I/O	–	H14
1	1016	I/O, DATA1 (1)	C13	A10
1	1017	I/O	–	J14
1	1018	I/O	–	K14
1	1019	I/O	A10	L14
1	1020	I/O	–	B13
1	1021	I/O	E14	C13
–	1022	VCCIO	VCCIO1	VCCIO1
1	1023	I/O	–	D13
1	1024	I/O	B11	E13
1	1025	I/O	C12	F13
1	1026	I/O	D13	G13
1	1027	I/O	E13	H13
1	1028	I/O	A9	J13
1	1029	I/O	B10	K13
1	1030	I/O	–	L13
1	1031	I/O	C11	E12
1	1032	I/O	–	–
1	1033	I/O, DATA2 (1)	A8	A9
–	1034	GNDIO	GND	GND
–	1035	GNDINT	GND	GND
–	1036	GNDINT	GND	GND
–	1037	VCCINT	VCCINT	VCCINT
–	1038	VCCINT	VCCINT	VCCINT
1	1039	I/O	B9	F12
1	1040	I/O	–	–
1	1041	I/O	C10	G12
1	1042	I/O	–	H12
1	1043	I/O	D11	J12
1	1044	I/O	A7	K12
1	1045	I/O	B8	L12
1	1046	I/O	E11	E11
1	1047	I/O	C9	F11
1	1048	I/O	D10	G11
1	1049	I/O	–	H11
–	1050	VCCIO	VCCIO1	VCCIO1
1	1051	I/O	A6	J11
1	1052	I/O	–	K11
1	1053	I/O, DATA3 (1)	B7	A8

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	1,020-Pin FineLine BGA
1	1054	I/O	–	L11
1	1055	I/O	–	B10
1	1056	I/O	C8	C10
1	1057	I/O	–	D10
1	1058	I/O	E10	E10
1	1059	I/O	–	F10
1	1060	I/O	D9	G10
–	1061	GNDIO	GND	GND
1	1062	I/O	A5	H10
1	1063	I/O	B6	J10
1	1064	I/O	C7	K10
1	1065	I/O	D8	L10
1	1066	I/O	A4	B9
1	1067	I/O	–	C9
1	1068	I/O	E9	D9
1	1069	I/O	–	E9
1	1070	I/O, DATA4 (1)	B5	B5
1	1071	I/O	–	F9
–	1072	VCCIO	VCCIO1	VCCIO1
1	1073	I/O	–	G9
1	1074	I/O	A3	H9
1	1075	I/O	–	J9
1	1076	I/O	C6	K9
1	1077	I/O	–	L9
1	1078	I/O	D7	B8
1	1079	I/O	E8	C8
1	1080	I/O	B4	D8
1	1081	I/O	A2	E8
1	1082	I/O	C5	F8
–	1083	GNDIO	GND	GND
1	1084	I/O	B3	G8
1	1085	I/O	–	H8
1	1086	I/O	D6	E7
1	1087	I/O	–	F7
1	1088	I/O, DATA5 (1)	E7	A5
1	1089	–	–	–

Pin Name	652-Pin BGA	1,020-Pin FineLine BGA
MSEL0 (5)	U35	J30
MSEL1 (5)	W35	K30
nSTATUS (5)	AN17	AM14
nCONFIG (5)	W32	R30
DCLK (5)	U3	W3
CONF_DONE (5)	AM17	AM13
INIT_DONE (3)	C16	A15
nCE (5)	U1	AC3
nCEO (5)	C19	A23
nWS (1)	M1	C4
nRS (1)	N1	D4
nCS (1)	P2	D3
CS (1)	R2	E3
RDYnBSY (1)	A14	A14
CLKUSR (1)	C15	A13
DATA7 (1)	M6	B4
DATA6 (1)	L6	A4
DATA5 (1)	E7	A5
DATA4 (1)	B5	B5
DATA3 (1)	B7	A8
DATA2 (1)	A8	A9
DATA1 (1)	C13	A10
DATA0 (5), (6)	U4	V3
TDI (5)	W1	AD3
TDO (5)	C17	A18
TCK (5)	AN19	AM19
TMS (5)	AM19	AM20
TRST (5)	D19	A24
Dedicated Fast I/Os	B19, B17, AP19, AP17	A20, A19, AM18, AM15,
CLK1p	W34	N30
CLK2p	U2	Y3
CLK3p	Y34	W30
CLK4p	T2	P3
LOCK1 (9)	AA30	AC30
LOCK2 (9)	AB6	AK4
LOCK3 (9)	R31	H30
LOCK4 (9)	AC6	AK5
CLKLK_ENA (5), (10)	W33	P30
CLKLK_OUT1p (8)	U31	AM29
CLKLK_OUT2p (8)	Y3	AH3
CLKLK_FB1p (8)	Y32	AL28
CLKLK_FB2p	T4	K3
DEV_CLRn (3)	T6	H3
DEV_OE (3)	Y5	AE3

Pin Name	652-Pin BGA	1,020-Pin FineLine BGA
VCCINT	A17, A19, AA31, AA4, AC3, AC32, AE2, AE33, AG1, AH31, AH35, AH4, AK33, AL12, AL2, AL24, AM12, AM24, AR17, AR19, D12, D24, E12, E24, F3, F35, G30, H1, H5, K31, L3, M30, N35, N4, R34, R5, U34, U5, W3, W31	A2, B1, F1, F2, L1, L2, U1, U2, U3, AB1, AB2, AG1, AG2, AL1, AM2, AL6, AM6, AL11, AM11, AL17, AM17, AL22, AM22, AL27, AM27, AM31, AL32, AG31, AG32, AB31, AB32, T30, T31, T32, L31, L32, F31, F32, B32, A31, A27, B27, A22, B22, A16, B16, A11, B11, A6, B6
VCCIO1	C4, D5, E17	A12, B12, A7, B7, A3
VCCIO2	E19, D31, C32	A30, A26, B26, A21, B21
VCCIO3	F30, F31, U30	M31, M32, G31, G32, C32
VCCIO4	W30, AL31, AL32	AK32, AF31, AF32, AA31, AA32
VCCIO5	AN32, AN33, AL19	AL21, AM21, AL26, AM26, AM30
VCCIO6	AL17, AM5, AN4	AM3, AL7, AM7, AL12, AM12
VCCIO7	AL3, AL4, W6	AA1, AA2, AF1, AF2,AK1
VCCIO8	U6, E3, E4	C1, G1, G2, M1, M2
VCC_CKLK1 (2)	AA35	W24
VCC_CKLK2 (2)	W4	Y9
VCC_CKLK3 (2)	T34	M24
VCC_CKLK4 (2)	R4	P9
VCC_CKOUT1 (7)	U33	N24
VCC_CKOUT2 (7)	Y1	AA9
GND	A1, A18, A35, AK18, AL18, AL30, AL5, AL6, AM18, AM2, AM3, AM31, AM32, AM33, AM34, AM4, AN1, AN18, AN2, AN3, AN34, AN35, AP1, AP18, AP2, AP34, AP35, AR1, AR18, AR35, B1, B18, B2, B34, B35, C18, C2, C3, C33, C34, C35, D18, D2, D3, D17, D32, D33, D34, D4, E18, E30, E31, E32, E33, E5, E6, F18, V1, V2, V3, V30, V31, V32, V33, V34, V4, V5, V6	B2, B3, C2, C3, F3, F4, G3, G4, L3, L4, M3, M4, T1, T2, T3, AA3, AA4, AB3, AB4, AF3, AF4, AG3, AG4, AK2, AK3, AL2, AL3, AJ6, AJ7, AK6, AK7, AJ11, AJ12, AK11, AK12, AL16, AM16, AJ21, AJ22, AK21, AK22, AJ26, AJ27, AK26, AK27, AK30, AK31, AL30, AL31, AG29, AG30, AF29, AF30, AB29, AB30, AA29, AA30, U30, U31, U32, M29, M30, L29, L30, G29, G30, F29, F30, C30, C31, B30, B31, C26, C27, D26, D27, C21, C22, D21, D22, A17, B17, C11, C12, D11, D12, C6, C7, D6, D7
GND_CKLK1 (2)	Y30	V24
GND_CKLK2 (2)	W2	V9
GND_CKLK3 (2)	T33, V35	P23, P24
GND_CKLK4 (2)	R3	T9
GND_CKOUT1 (7)	U32	T24
GND_CKOUT2 (7)	Y2	W9
No Connect (N.C.)	–	–
Total User I/O Pins (11)	488	808

Notes:

(1) This pin can be used as a user I/O pin after configuration.

(2) This pin is the power or ground for the ClockLock and ClockBoost circuitry. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device. VCC_CKLK has the same voltage specifications as the VCCINT and should be connected to a 1.8-V power supply. If the ClockLock or ClockBoost circuitry is not used, this power or ground pin should be connected to VCCINT or GNDINT, respectively.

(3) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.

(4) This pin is the complementary signal for the LVDS pair on dedicated inputs and outputs that can be configured for the LVDS standard. If not used for the LVDS pair, these pins are regular I/O pins. Pins with the "n" suffix carry the negative signal for the LVDS channel. Pins with a "p" suffix carry the positive signal for the LVDS channel.

(5) This pin is a dedicated pin; it is not available as a user I/O pin.

(6) This pin is tri-stated in user mode.

(7) This pin is the power or ground for the external output of a PLL. These pins should be set to the VCCIO level/standard desired for the external clock ouput. To ensure noise resistance, the power and ground supply to the PLL external output should be isolated from the power and ground to the rest of the VCCIO and GNDIO pins. If the PLL or external output is not used, this power or ground pin should be connected to VCCIO or GNDIO, respectively.

(8) The CLKLK_OUT pin is powered by the VCC_CKOUT and GND_CKOUT pins.

(9) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry is locked to the incoming clock and generates an internal clock, LOCK is driven high. LOCK remains high if a periodic clock stops clocking. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.

(10) This pin is the active high enable pin for all of the PLL circuits in the device. When de-asserted, all PLLs are reset to their default, unlocked state and will stop clocking. Once re-asserted, the PLLs will lock again and start clocking. If this pin function is not needed, the pin should be connected to VCCINT.

(11) The user I/O pin count includes dedicated inputs and dedicated clock inputs. It does not include the dedicated clock feedback and output pins.

Pin Name (1)	**208-Pin RQFP** (2)	**240-Pin RQFP** (3)	**356-Pin FineLine BGA**	**484-Pin FineLine BGA**
MSEL0 (2)	25	29	P1	L19
MSEL1 (2)	26	30	P2	L18
nSTATUS (2)	82	92	AF15	W11
nCONFIG (2)	29	33	R1	M19
DCLK (2)	132	152	N25	L5
CONF_DONE (2)	83	93	AE15	W10
INIT_DONE (3)	178	206	A16	G13
nCE (2)	130	150	P26	M4
nCEO (2)	185	213	A12	E12
nWS (4)	145	164	H22	M7
nRS (4)	142	161	H24	L8
nCS (4)	141	160	J24	K7
CS (4)	138	157	K25	P4
RDYnBSY (4)	177	205	B16	G12
CLKUSR (4)	176	204	C16	H12
DATA7 (4)	146	166	G23	K8
DATA6 (4)	150	169	F24	J6
DATA5 (4)	157	181	C24	D4
DATA4 (4)	160	185	A25	E7
DATA3 (4)	163	189	B22	D8
DATA2 (4)	168	195	B20	G10
DATA1 (4)	173	200	B18	H11
DATA0 (2), (5)	133	153	M26	L4
TDI (2)	129	149	P25	M5
TDO (2)	180	208	B15	E11
TCK (2)	76	87	AE12	W12
TMS (2)	75	86	AF11	W13
TRST (2)	186	214	B12	D12
Dedicated Inputs	81, 77, 181, 184	91, 88, 209, 212	A13, A15, AF12, AE14	D11, F12, V11, V12
Dedicated Clock Pins	27, 131	31, 151	P3, N26	L6, M18
LOCK (6)	119	138	T24	R4
CLK2 (7)	131	151	N26	L6
DEV_CLRn (3)	137	156	L23	N7
DEV_OE (3)	124	143	R26	N6
VCCINT	1, 3, 11, 23, 28, 36, 48, 52, 79, 105, 109, 121, 126, 148, 154, 156, 182	1, 5, 14, 27, 32, 39, 52, 60, 90, 122, 127, 140, 145, 168, 176, 179, 210	A14, AB25, AB3, AF13, AF14, B14, E23, E1, H1, J23, L1,M25, P4, R2, T22, U4, Y26	AA1, AA22, B1, B22, H9, J8, J13, K11, K14, L10, M13, M14, M22, N9, N12, P10, P15, R7, R14
VCCIO	8, 53, 80, 86, 136, 172, 189, 208	12, 45, 67, 97, 120, 148, 177, 199, 229	C26, M22, P22, AD26, AF26, AD14, AD12, AF1, AD1, P5, M5, C1, A1, C12, C14, A26	G8, H7, H14, J10, J15, K9, K12, L1, L13, L22, M10, N11, N14, P8, P13, R9, R16, T8, T15
VCC_CKLK (8)	125	144	P23	L9

Pin Name (1)	**208-Pin RQFP** (2)	**240-Pin RQFP** (3)	**356-Pin FineLine BGA**	**484-Pin FineLine BGA**
GNDINT	4, 12, 16, 24, 35, 39, 47, 78, 110, 118, 127, 143, 147, 153, 183	6, 15, 19, 28, 38, 42, 51, 89, 128, 137, 146, 162, 167, 175, 211	AB4, AB5, AC3, AC22, AC23, AC24, AD2, AD13, AD25, AE1, AE13, AE26, B1, B13, B26, C2, C13, C25, D3, D4, D22, D23, D24, E5, N3, N4, N5, N22, N23, N24	A1, A11, A22, AA2, AA21, AB1, AB11, AB22, B2, B21, F6, F17, G7, G16, H8, H15, J9, J11, J14, K10, K13, L2, L11, L12, M1, M11, M12, M21, N10, N13, P9, P14, R8, R15, T7, T16, U6, U17
GNDIO (9)	10, 43, 64, 95, 114, 149, 169, 199	26, 56, 78, 108, 132, 165, 188, 218, 240	–	–
GND_CKLK (8)	128	147	P24	M9
No Connect (N.C.)	–	–	–	A9, A10, A12, A13, A14, AB9, AB10, AB12, AB13, AB14
Total User I/O Pins (10)	144	174	277	382

Notes:

(1) All pins that are not listed are user I/O pins.
(2) This pin is a dedicated pin; it is not available as a user I/O pin.
(3) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.
(4) This pin can be used as a user I/O pin after configuration.
(5) This pin is tri-stated in user mode.
(6) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry is locked to the incoming clock and generates an internal clock, LOCK is driven high. LOCK remains high if a periodic clock stops clocking. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.
(7) This pin drives the ClockLock and ClockBoost circuitry.
(8) This pin is the power or ground for the ClockLock and ClockBoost circuitry. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device. VCC_CKLK has the same voltage specifications as the VCCINT and should be connected to a 2.5-V power supply. If the ClockLock or ClockBoost circuitry is not used, this power or ground pin should be connected to VCCINT or GNDINT, respectively.
(9) GNDIO and GNDINT are connected together in BGA packages.
(10) The user I/O pin count includes dedicated inputs, dedicated clock inputs, and all I/O pins.

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin PQFP (1)	240-Pin PQFP (1)	484-Pin FineLine BGA	356-Pin BGA	652-Pin BGA	672-Pin FineLine BGA
8	1	I/O	–	–	B11	–	F6	E5
8	2	I/O	155	180	B10	D25	F5	E3
8	3	I/O	–	–	B9	–	F4	F5
8	4	I/O	–	–	A8	E22	C1	F4
–	5	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
8	6	I/O	–	–	B8	–	D1	E4
8	7	I/O	–	–	A7	–	E2	F3
8	8	I/O	152	178	B7	E24	G6	D5
8	9	I/O	–	–	B6	–	G5	G5
8	10	I/O	–	–	A6	D26	G4	G3
–	11	VCCIO	VCCIO8	VCCIO8	VCCIO8	VCCIO8	VCCIO8	VCCIO8
8	12	I/O	–	174	A5	–	G3	G8
8	13	I/O	–	–	B5	–	F2	G4
8	14	I/O	151	173	B4	F22	E1	C4
8	15	I/O	–	–	A3	–	G2	G6
8	16	I/O	–	–	A4	E25	H6	H5
–	17	GNDINT	GND	GND	GND	GND	GND	GND
8	18	I/O	–	172	C3	–	H4	G7
8	19	I/O	–	–	C1	–	H3	H7
8	20	I/O	–	171	D3	F23	F1	H4
8	21	I/O	–	–	D2	–	H2	H6
8	22	I/O	–	–	C2	E26	G1	K7
–	23	GNDIO	GND	GND	GND	GND	GND	GND
8	24	I/O	–	170	D1	–	J6	J5
8	25	I/O	–	–	B3	–	J5	H9
8	26	I/O, DATA6 (2)	150	169	J6	F24	L6	L8
8	27	I/O	–	–	E3	–	J4	H3
8	28	I/O	–	–	E1	G22	J3	K3
–	29	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
8	30	I/O	–	–	E6	–	J2	J4
8	31	I/O	–	–	E2	–	J1	K5
8	32	I/O, DATA7 (2)	146	166	K8	G23	M6	M10
8	33	I/O	–	–	A2	–	K6	L6
8	34	I/O	–	–	E4	F25	K5	J7
–	35	VCCIO	VCCIO8	VCCIO8	VCCIO8	VCCIO8	VCCIO8	VCCIO8
8	36	I/O	–	–	F3	F26	K4	J3
8	37	I/O	–	–	E5	–	K3	K8
8	38	I/O, nWS (2)	145	164	M7	H22	M1	P9
8	39	I/O	–	–	F5	–	K2	K6
8	40	I/O	–	–	F2	G24	K1	K4
–	41	GNDINT	GND	GND	GND	GND	GND	GND
8	42	I/O	–	–	F4	H23	L5	N5
8	43	I/O	–	–	H5	–	L4	M8
8	44	I/O	144	163	G3	G25	L2	J8
8	45	I/O	–	–	F7	–	L1	M6
8	46	I/O	–	–	G6	G26	M5	L7
–	47	GNDIO	GND	GND	GND	GND	GND	GND

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin PQFP (1)	240-Pin PQFP (1)	484-Pin FineLine BGA	356-Pin BGA	652-Pin BGA	672-Pin FineLine BGA
8	48	I/O	–	–	F1	J22	M4	L9
8	49	I/O	–	–	H1	–	M3	M7
8	50	I/O, nRS (2)	142	161	L8	H24	N1	N10
8	51	I/O	–	–	G2	–	M2	L5
8	52	I/O	–	–	H3	H25	N6	P8
–	53	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
8	54	I/O	–	–	G4	H26	N5	L4
8	55	I/O	–	–	J4	–	N3	L3
8	56	I/O, nCS (2)	141	160	K7	J24	P2	M9
8	57	I/O	–	–	G5	–	N2	R4
8	58	I/O	–	–	G1	K22	P6	M5
–	59	VCCIO	VCCIO8	VCCIO8	VCCIO8	VCCIO8	VCCIO8	VCCIO8
8	60	I/O	–	–	H6	J25	P5	M3
8	61	I/O	–	–	H4	–	P4	P4
8	62	I/O	–	–	H2	K23	P3	J6
8	63	I/O	–	–	L3	–	P1	R3
8	64	I/O	–	–	K6	J26	R6	P5
–	65	GNDINT	GND	GND	GND	GND	GND	GND
–	66	VCC_CKLK4 (3)	140	159	M8	K24	R4	P10
–	67	GND_CKLK4 (3)	139	158	N8	L22	R3	R10
–	68	GND_CKLK4 (3)	139	158	N8	L22	R3	R10
8	69	I/O, CS (2)	138	157	P4	K25	R2	T6
8	70	I/O	–	–	K4	K26	R1	M4
8	71	I/O, DEV_CLRn (4)	137	156	N7	L23	T6	R9
–	72	VCCIO	VCCIO8	VCCIO8	–	VCCIO8	VCCIO8	–
–	73	GNDIO	GND	GND	GND	GND	GND	GND
8	74	I/O, CLKLK_FB2n (5)	–	–	P6	L24	T5	T8
–	75	CLKLK_FB2p	135	155	R6	L25	T4	U8
8	76	I/O, CLK4n (5)	–	–	N5	L26	T3	R7
–	77	CLK4p	134	154	N4	M23	T2	R6
8	78	I/O, CLK2n (5)	–	–	L7	M24	T1	N9
–	79	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
–	80	DATA0 (6), (7)	133	153	L4	M26	U4	N6
–	81	DCLK (6)	132	152	L5	N25	U3	N7
–	82	CLK2p	131	151	L6	N26	U2	N8
–	83	NCE (6)	130	150	M4	P26	U1	P6
–	84	TDI (6)	129	149	M5	P25	W1	P7
–	85	VCCIO	VCCIO7	VCCIO7	–	VCCIO7	VCCIO7	–
–	86	GND_CKLK2 (3)	128	147	M9	P24	W2	P11
–	87	GND_CKLK2 (3)	128	147	M9	P24	W2	P11
–	88	GNDINT	GND	GND	GND	GND	GND	GND
–	89	VCC_CKLK2 (3)	125	144	L9	P23	W4	N11
7	90	I/O, DEV_OE (4)	124	143	N6	R26	Y5	R8
–	91	VCC_CKOUT2 (8)	123	142	T5	R25	Y1	V7

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin PQFP (1)	240-Pin PQFP (1)	484-Pin FineLine BGA	356-Pin BGA	652-Pin BGA	672-Pin FineLine BGA
–	92	GND_CKOUT2 (8)	122	141	T4	R24	Y2	V6
–	93	CLKLK_OUT2p (9)	120	139	P5	R23	Y3	T7
7	94	I/O, CLKLK_OUT2n (5)	–	–	R5	R22	Y4	U7
–	95	VCCIO	VCCIO7	VCCIO7	VCCIO7	VCCIO7	VCCIO7	VCCIO7
7	96	I/O	–	–	J5	T26	W5	D1
7	97	I/O	–	–	J7	T25	Y6	D2
7	98	I/O, LOCK2 (10)	119	138	R4	T24	AB6	U6
7	99	I/O	–	–	K5	T23	AA2	E1
7	100	I/O	–	–	J3	U26	AA3	E2
–	101	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
7	102	I/O	–	–	M6	U25	AA5	F1
7	103	I/O	–	–	J2	–	AA6	F2
7	104	I/O	–	–	J1	U24	AB1	R5
7	105	I/O	–	–	N2	–	AB2	G1
7	106	I/O	–	–	K3	V26	AB3	G2
–	107	GNDIO	GND	GND	GND	GND	GND	GND
7	108	I/O	117	136	K1	U23	AB4	H1
7	109	I/O	–	–	M2	–	AB5	H2
7	110	I/O, LOCK4 (10)	116	135	U5	V25	AC6	W7
7	111	I/O	–	–	N1	–	AC1	J1
7	112	I/O	–	–	M3	U22	AC2	J2
–	113	GNDINT	GND	GND	GND	GND	GND	GND
7	114	I/O	–	–	K2	V24	AC4	K1
7	115	I/O	–	–	N3	–	AC5	K2
7	116	I/O	–	134	P3	W26	AA1	T5
7	117	I/O	–	–	P1	–	AD1	L1
7	118	I/O	–	–	R3	V23	AD2	L2
–	119	VCCIO	VCCIO7	VCCIO7	VCCIO7	VCCIO7	VCCIO7	VCCIO7
7	120	I/O	–	–	P2	W25	AD3	M1
7	121	I/O	–	–	R2	–	AD4	M2
7	122	I/O	–	–	R1	V22	AD5	T3
7	123	I/O	–	133	T1	–	AD6	R1
7	124	I/O	–	–	U3	W24	AE1	R2
–	125	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
7	126	I/O	–	–	U4	W23	AE3	T1
7	127	I/O	–	–	T3	–	AE4	T2
7	128	I/O	–	131	T2	Y25	AE5	U5
7	129	I/O	–	–	U2	–	AE6	U1
7	130	I/O	–	130	U1	Y24	AF1	U2
–	131	GNDIO	GND	GND	GND	GND	GND	GND
7	132	I/O	–	–	V3	W22	AF2	V1
7	133	I/O	–	–	Y3	–	AF3	V2
7	134	I/O	113	129	W3	AA26	AF4	T4
7	135	I/O	–	–	V4	–	AF5	W1

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin PQFP (1)	240-Pin PQFP (1)	484-Pin FineLine BGA	356-Pin BGA	652-Pin BGA	672-Pin FineLine BGA
7	136	I/O	–	–	W4	AA25	AF6	W2
–	137	GNDINT	GND	GND	GND	GND	GND	GND
7	138	I/O	–	–	W5	Y23	AH1	Y1
7	139	I/O	–	–	Y4	–	AG2	Y2
7	140	I/O	112	126	Y2	AA24	AG3	U4
7	141	I/O	–	–	W2	–	AG4	AA1
7	142	I/O	–	–	AA3	Y22	AG5	AA2
–	143	VCCIO	VCCIO7	VCCIO7	VCCIO7	VCCIO7	VCCIO7	VCCIO7
7	144	I/O	–	–	V2	AA23	AG6	AB1
7	145	I/O	–	–	Y1	–	AJ1	AB2
7	146	I/O	111	125	V1	AB26	AH2	W4
7	147	I/O	–	–	AB2	–	AK1	AC1
7	148	I/O	–	–	W1	–	AH3	AC2
–	149	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
7	150	I/O	–	–	AB3	AA22	AH5	U3
7	151	I/O	–	–	AB4	–	AH6	V3
7	152	I/O	108	124	AA4	AB24	AJ2	W5
7	153	I/O	–	–	AA5	–	AL1	W6
7	154	I/O	–	–	AB5	–	AK2	V5
–	155	GNDIO	GND	GND	GND	GND	GND	GND
7	156	I/O	–	–	AA6	AC26	AJ3	V4
7	157	I/O	–	–	AB6	–	AJ4	W3
7	158	I/O	107	123	AA7	AB23	AJ5	Y5
7	159	I/O	–	–	AB7	–	AJ6	AB5
7	160	I/O	–	–	AA8	–	AM1	AA5
–	161	GNDINT	GND	GND	GND	GND	GND	GND
7	162	I/O	–	–	AA11	AC25	AK3	Y6
7	163	I/O	–	–	AA10	–	AK4	AA6
7	164	I/O	106	121	AB8	AB22	AK5	AA7
7	165	I/O	–	–	AA9	–	AK6	AB6
–	166	VCCIO	VCCIO7	VCCIO7	VCCIO7	VCCIO7	VCCIO7	–
–	167	VCCIO	VCCIO6	VCCIO6	VCCIO6	VCCIO6	VCCIO6	VCCIO6
6	168	I/O	104	119	Y5	AD24	AR8	AB7
6	169	I/O	–	118	V5	AE25	AN11	Y7
6	170	I/O	103	117	Y6	AD23	AP10	AB8
6	171	I/O	102	116	T6	AD22	AR9	V8
6	172	I/O	–	–	P7	AF25	AL13	T9
6	173	I/O	101	115	W7	AE24	AM13	AA9
6	174	I/O	–	–	W6	AE23	AN12	AA8
6	175	I/O	100	114	V6	AD21	AP11	Y8
6	176	I/O	99	113	V7	AF24	AL14	Y9
6	177	I/O	–	112	U7	AE22	AR10	W9
–	178	GNDIO	GND	GND	GND	GND	GND	GND
6	179	I/O	98	111	Y7	AF23	AN13	AB9
6	180	I/O	97	110	U8	AD20	AP12	W10
6	181	I/O	96	109	V8	AF22	AM14	Y10
6	182	I/O	–	–	W8	AE21	AR11	AA10

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin PQFP (1)	240-Pin PQFP (1)	484-Pin FineLine BGA	356-Pin BGA	652-Pin BGA	672-Pin FineLine BGA
6	183	I/O	94	107	Y9	AF21	AL15	AB11
6	184	I/O	–	106	T9	AD19	AN14	V11
6	185	I/O	93	105	Y8	AE20	AP13	AB10
6	186	I/O	–	104	W9	AF20	AR12	AA11
6	187	I/O	92	103	V9	AD18	AR13	Y11
6	188	I/O	–	–	U9	AE19	AM15	W11
–	189	VCCIO	VCCIO6	VCCIO6	VCCIO6	VCCIO6	VCCIO6	VCCIO6
6	190	I/O	91	102	T10	AF19	AN15	V12
6	191	I/O	90	101	U10	AE18	AL16	W12
6	192	I/O	–	–	V10	AD17	AP14	Y12
6	193	I/O	89	100	P11	AF18	AR14	T13
6	194	I/O	88	99	U12	AE17	AP15	W14
6	195	I/O	87	98	Y10	AD16	AR15	AB12
–	196	VCCIO	VCCIO6	VCCIO6	–	VCCIO6	VCCIO6	VCCIO6
6	197	I/O	85	96	R11	AF17	AM16	U13
6	198	I/O	84	95	R10	AE16	AN16	U12
6	199	I/O	–	–	U11	AF16	AP16	W13
6	200	I/O	–	94	T11	AD15	AR16	V13
–	201	CONF_DONE (6)	83	93	W10	AE15	AM17	AA12
–	202	NSTATUS (6)	82	92	W11	AF15	AN17	AA13
5	203	FAST4	81	91	V11	AE14	AP17	Y13
–	204	VCCIO	VCCIO5	VCCIO5	–	VCCIO5	VCCIO5	VCCIO5
–	205	GNDINT	GND	GND	GND	GND	GND	GND
–	206	GNDINT	GND	GND	GND	GND	GND	GND
–	207	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
–	208	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
–	209	GNDINT	GND	GND	GND	GND	GND	GND
–	210	GNDINT	GND	GND	GND	GND	GND	GND
–	211	GNDIO	GND	GND	GND	GND	GND	GND
5	212	FAST3	77	88	V12	AF12	AP19	Y14
–	213	TCK (6)	76	87	W12	AE12	AN19	AA14
–	214	TMS (6)	75	86	W13	AF11	AM19	AA15
5	215	I/O	74	85	Y11	AE11	AR20	AB13
5	216	I/O	73	84	T12	AF10	AP20	V14
5	217	I/O	–	83	Y12	AD11	AN20	AB14
5	218	I/O	72	82	V13	AE10	AM20	Y15
5	219	I/O	–	–	R12	AF9	AR21	U14
5	220	I/O	71	81	T13	AD10	AP21	V15
5	221	I/O	–	80	Y13	AE9	AR22	AB15
5	222	I/O	70	79	U13	AF8	AP22	W15
5	223	I/O	69	77	Y14	AD9	AL20	AB16
5	224	I/O	68	76	P12	AE8	AN21	T14
–	225	VCCIO	VCCIO5	VCCIO5	VCCIO5	VCCIO5	VCCIO5	VCCIO5
5	226	I/O	67	75	W14	AF7	AM21	AA16
5	227	I/O	66	74	V14	AE7	AR23	Y16
5	228	I/O	–	–	U14	AD8	AR24	W16
5	229	I/O	65	73	R13	AF6	AP23	U15

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin PQFP (1)	240-Pin PQFP (1)	484-Pin FineLine BGA	356-Pin BGA	652-Pin BGA	672-Pin FineLine BGA
5	230	I/O	–	–	Y15	AE6	AN22	AB17
5	231	I/O	63	72	T14	AD7	AL21	V16
5	232	I/O	62	71	W15	AF5	AR25	AA17
5	233	I/O	–	70	Y16	AE5	AM22	AB18
5	234	I/O	61	69	V15	AD6	AP24	Y17
5	235	I/O	60	68	W16	AF4	AN23	AA18
–	236	GNDIO	GND	GND	GND	GND	GND	GND
–	237	VCCIO	VCCIO5	VCCIO5	–	VCCIO5	VCCIO5	VCCIO5
5	238	I/O	59	66	U15	AE4	AR26	W17
5	239	I/O	–	–	V16	AF3	AL22	Y18
5	240	I/O	58	65	U16	AD5	AP25	W18
5	241	I/O	–	–	W17	AE3	AN24	AA19
5	242	I/O	57	64	V17	AF2	AM23	Y19
5	243	I/O	–	–	U18	AD4	AL23	W20
5	244	I/O	56	63	V18	AE2	AR27	Y20
5	245	I/O	55	62	Y18	AD3	AP26	AB20
5	246	I/O	–	–	Y17	AC5	AN25	AB19
5	247	I/O	54	61	W18	AC4	AR28	AA20
–	248	VCCIO	VCCIO5	VCCIO5	VCCIO5	VCCIO5	VCCIO5	VCCIO5
–	249	VCCIO	VCCIO4	VCCIO4	VCCIO4	VCCIO4	VCCIO4	VCCIO4
4	250	I/O	–	–	AA12	–	AL33	AA21
4	251	I/O	51	59	AB15	AA5	AK30	Y22
4	252	I/O	–	–	AB16	–	AK31	AB21
4	253	I/O	–	–	AA13	AC2	AK32	U19
–	254	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
4	255	I/O	–	–	AB17	–	AL34	AB22
4	256	I/O	–	–	AA14	–	AM35	V19
4	257	I/O	50	58	AA15	AC1	AJ30	T18
4	258	I/O	–	–	AB18	–	AJ31	W21
4	259	I/O	–	57	AA16	AA4	AJ32	V20
–	260	GNDIO	GND	GND	GND	GND	GND	GND
4	261	I/O	–	–	AB19	–	AJ33	V21
4	262	I/O	–	–	AB20	–	AK34	Y21
4	263	I/O	49	–	AA17	AB2	AL35	W22
4	264	I/O	–	55	AA18	–	AJ34	AA22
4	265	I/O	–	–	AB21	Y5	AH30	U20
–	266	GNDINT	GND	GND	GND	GND	GND	GND
4	267	I/O	–	–	Y22	AB1	AH32	R17
4	268	I/O	–	–	AA20	–	AH33	W23
4	269	I/O	46	54	AA19	AA3	AK35	T19
4	270	I/O	–	–	V21	–	AH34	U21
4	271	I/O	–	–	V22	Y4	AJ35	P17
–	272	VCCIO	VCCIO4	VCCIO4	VCCIO4	VCCIO4	VCCIO4	VCCIO4
4	273	I/O	–	–	W21	AA2	AG30	R18
4	274	I/O	–	–	W22	–	AG31	W24
4	275	I/O	45	53	Y21	AA1	AG32	T20
4	276	I/O	–	–	W19	–	AG33	V24

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin PQFP (1)	240-Pin PQFP (1)	484-Pin FineLine BGA	356-Pin BGA	652-Pin BGA	672-Pin FineLine BGA
4	277	I/O	–	–	V20	W5	AG34	N16
–	278	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
4	279	I/O	–	50	Y19	Y3	AG35	V22
4	280	I/O	–	–	R17	–	AF30	R19
4	281	I/O	44	49	Y20	W4	AF31	V23
4	282	I/O	–	–	T17	–	AF32	P18
4	283	I/O	–	–	P16	Y2	AF33	N17
–	284	GNDIO	GND	GND	GND	GND	GND	GND
4	285	I/O	–	–	U19	Y1	AF34	T21
4	286	I/O	–	–	T18	–	AF35	R21
4	287	I/O	–	48	T19	V5	AE30	U22
4	288	I/O	–	–	V19	–	AE31	R20
4	289	I/O	–	–	U20	W3	AE32	P22
–	290	GNDINT	GND	GND	GND	GND	GND	GND
4	291	I/O	–	–	W20	V4	AE34	N18
4	292	I/O	–	–	R18	–	AE35	U23
4	293	I/O	–	47	N15	W2	AD30	N19
4	294	I/O	–	–	U21	–	AD31	N22
4	295	I/O	–	46	P17	W1	AD32	L20
–	296	VCCIO	VCCIO4	VCCIO4	VCCIO4	VCCIO4	VCCIO4	VCCIO4
4	297	I/O	–	–	R19	V3	AD33	M17
4	298	I/O	–	–	M15	–	AD34	T22
4	299	I/O	41	44	N16	U5	AD35	M18
4	300	I/O	–	–	U22	–	AC30	T23
4	301	I/O	40	43	P18	V2	AC31	R23
–	302	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
4	303	I/O	–	–	T22	V1	AC33	U24
4	304	I/O	–	–	L14	–	AC34	R24
4	305	I/O	38	41	T20	U3	AC35	T24
4	306	I/O	–	–	N17	–	AB30	M21
4	307	I/O	–	–	T21	T5	AB31	M24
–	308	GNDIO	GND	GND	GND	GND	GND	GND
4	309	I/O	–	–	M16	U2	AB32	M22
4	310	I/O	–	–	L15	–	AB33	R22
4	311	I/O	37	40	P19	T4	AB34	M23
4	312	I/O	–	–	N19	–	AB35	L22
4	313	I/O	–	–	R20	U1	AA30	L21
–	314	GNDINT	GND	GND	GND	GND	GND	GND
4	315	I/O	–	–	N18	–	AA32	L23
4	316	I/O	–	–	M20	T3	AA33	L24
4	317	I/O	–	–	L16	–	AA34	N23
4	318	I/O	34	37	R21	T2	AA35	AF18
4	319	I/O	33	36	L17	R5	Y30	AE18
–	320	VCCIO	VCCIO4	VCCIO4	VCCIO4	VCCIO4	VCCIO4	–
4	321	I/O	–	–	L20	–	Y31	AF20
4	322	I/O	32	35	J18	–	Y32	AE20
4	323	I/O, CLK3n (5)	–	–	K18	T1	Y33	M20

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin PQFP (1)	240-Pin PQFP (1)	484-Pin FineLine BGA	356-Pin BGA	652-Pin BGA	672-Pin FineLine BGA
–	324	CLK3p	31	34	K17	R4	Y34	M19
4	325	I/O, CLK1n (5)	30	–	M17	R3	Y35	P19
–	326	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
–	327	nCONFIG (6)	29	33	M19	R1	W32	P21
–	328	CLKLK_ENA (6), (11)	28	32	M14	P4	W33	P16
–	329	CLK1p	27	31	M18	P3	W34	P20
–	330	MSEL1 (6)	26	30	L18	P2	W35	N20
–	331	MSEL0 (6)	25	29	L19	P1	U35	N21
–	332	GNDINT	GND	GND	GND	GND	GND	GND
3	333	I/O	22	25	K15	N2	U33	AF22
3	334	I/O	–	–	P20	–	U32	AE22
3	335	I/O	–	–	K16	N1	U31	AE23
3	336	I/O	–	–	P21	–	T35	AF23
3	337	I/O	–	–	N21	M1	T34	AC26
–	338	GNDIO	GND	GND	GND	GND	GND	GND
3	339	I/O	–	–	R22	M2	T33	AC25
3	340	I/O	–	–	N22	–	T32	AB25
3	341	I/O	21	24	P22	M3	T31	AB26
3	342	I/O	–	–	K19	–	T30	J23
3	343	I/O	–	–	K22	M4	R35	L19
–	344	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
3	345	I/O	20	23	K20	L2	R33	AA25
3	346	I/O	–	–	N20	–	R32	AA26
3	347	I/O	19	22	K21	L3	R31	L18
3	348	I/O	–	–	J20	–	R30	Y25
3	349	I/O	–	–	J19	L4	P35	Y26
–	350	VCCIO	VCCIO3	VCCIO3	VCCIO3	VCCIO3	VCCIO3	VCCIO3
3	351	I/O	18	21	J21	L5	P34	W25
3	352	I/O	–	–	J22	–	P33	W26
3	353	I/O	17	20	L21	K1	P32	J24
3	354	I/O	–	–	G21	–	P31	V25
3	355	I/O	–	–	J17	K2	P30	V26
–	356	GNDINT	GND	GND	GND	GND	GND	GND
3	357	I/O	15	18	J16	K3	N34	U25
3	358	I/O	–	–	G22	–	N33	U26
3	359	I/O	14	17	H19	J1	N32	K21
3	360	I/O	–	–	H21	–	N31	T25
3	361	I/O	–	–	H18	K4	N30	T26
–	362	GNDIO	GND	GND	GND	GND	GND	GND
3	363	I/O	–	–	H20	J2	M35	R25
3	364	I/O	–	–	H22	–	M34	R26
3	365	I/O	13	16	F22	K5	M33	K23
3	366	I/O	–	–	H17	–	M32	M25
3	367	I/O	–	–	G18	J3	M31	M26
–	368	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
3	369	I/O	–	–	E20	J4	L35	L25

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin PQFP (1)	240-Pin PQFP (1)	484-Pin FineLine BGA	356-Pin BGA	652-Pin BGA	672-Pin FineLine BGA
3	370	I/O	–	–	F18	–	L34	L26
3	371	I/O	9	13	F20	H2	L33	K20
3	372	I/O	–	–	G20	–	L32	K25
3	373	I/O	–	–	E22	J5	L31	K26
–	374	VCCIO	VCCIO3	VCCIO3	VCCIO3	VCCIO3	VCCIO3	VCCIO3
3	375	I/O	–	–	F19	H3	L30	J25
3	376	I/O	–	–	E19	–	K35	J26
3	377	I/O	7	11	G19	G1	K34	K22
3	378	I/O	–	–	D20	–	K33	H25
3	379	I/O	–	–	E18	H4	K32	H26
–	380	GNDINT	GND	GND	GND	GND	GND	GND
3	381	I/O	–	–	D19	G2	K30	G25
3	382	I/O	–	–	C20	–	J35	G26
3	383	I/O	–	10	C21	G3	H35	K24
3	384	I/O	–	–	B20	–	J34	F25
3	385	I/O	–	9	D22	H5	J33	F26
–	386	GNDIO	GND	GND	GND	GND	GND	GND
3	387	I/O	–	–	C22	F1	J32	E25
3	388	I/O	–	–	F21	–	J31	E26
3	389	I/O	–	8	A21	G4	J30	H24
3	390	I/O	–	–	E21	–	G35	D25
3	391	I/O	–	7	D21	F2	H34	D26
–	392	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
3	393	I/O	–	–	A20	F3	H33	K19
3	394	I/O	–	–	B19	–	H32	J20
3	395	I/O	6	4	A19	G5	H31	G22
3	396	I/O	–	–	B18	–	H30	H20
3	397	I/O	–	–	A18	F4	G34	H22
–	398	VCCIO	VCCIO3	VCCIO3	VCCIO3	VCCIO3	VCCIO3	VCCIO3
3	399	I/O	–	–	B17	E2	E35	J22
3	400	I/O	–	–	A17	–	F34	G24
3	401	I/O	5	3	B16	D1	G33	H21
3	402	I/O	–	–	A16	–	G32	G21
3	403	I/O	–	–	B15	E3	G31	J21
–	404	GNDINT	GND	GND	GND	GND	GND	GND
3	405	I/O	–	–	A15	F5	D35	F22
3	406	I/O	–	–	B14	D2	E34	G20
3	407	I/O	2	2	B13	E4	F33	F21
3	408	I/O	–	–	B12	–	F32	E22
–	409	VCCIO	VCCIO2	VCCIO2	–	VCCIO2	VCCIO2	VCCIO2
–	410	GNDIO	GND	GND	GND	GND	GND	GND
2	411	I/O	207	239	C19	B2	A28	E21
2	412	I/O	–	238	D18	C3	C25	F20
2	413	I/O	206	237	C18	D5	B26	E20
2	414	I/O	–	–	G17	A2	A27	J19
2	415	I/O	205	236	E17	C4	E23	G19
2	416	I/O	–	–	D17	B3	D23	F19

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin PQFP (1)	240-Pin PQFP (1)	484-Pin FineLine BGA	356-Pin BGA	652-Pin BGA	672-Pin FineLine BGA
2	417	I/O	204	235	C17	A3	C24	E19
2	418	I/O	–	–	H16	C5	B25	K18
2	419	I/O	203	234	F16	B4	E22	H18
2	420	I/O	202	233	E16	A4	A26	G18
–	421	VCCIO	VCCIO2	VCCIO2	VCCIO2	VCCIO2	VCCIO2	VCCIO2
2	422	I/O	201	232	C16	C6	C23	E18
2	423	I/O	200	231	D16	B5	B24	F18
2	424	I/O	198	230	C15	C7	D22	E17
2	425	I/O	–	–	D15	B6	A25	F17
–	426	VCCIO	VCCIO2	VCCIO2	–	VCCIO2	VCCIO2	VCCIO2
2	427	I/O	197	228	E15	A5	E21	G17
2	428	I/O	–	–	F15	C8	C22	H17
2	429	I/O	196	227	D14	B7	B23	F16
2	430	I/O	195	226	G15	A6	A24	J17
2	431	I/O	–	225	C14	A7	A23	E16
2	432	I/O	194	224	E14	B8	D21	G16
–	433	GNDIO	GND	GND	GND	GND	GND	GND
2	434	I/O	193	223	F14	C9	C21	H16
2	435	I/O	192	222	C13	A8	E20	E15
2	436	I/O	–	221	D13	B9	B22	F15
2	437	I/O	191	220	C12	C10	A22	E14
2	438	I/O	–	–	F13	A9	B21	H15
2	439	I/O	190	219	C11	B10	A21	E13
–	440	VCCIO	VCCIO2	VCCIO2	–	VCCIO2	VCCIO2	–
2	441	I/O	–	–	J12	C11	D20	L14
2	442	I/O	188	217	E13	A10	C20	G15
2	443	I/O	–	216	H13	B11	B20	K15
2	444	I/O	187	215	G14	A11	A20	J16
–	445	TRST (6)	186	214	D12	B12	D19	F14
–	446	NCEO (6)	185	213	E12	A12	C19	G14
1	447	FAST1	184	212	F12	A13	B19	H14
–	448	GNDINT	GND	GND	GND	GND	GND	GND
–	449	GNDINT	–	–	–	–	–	–
–	450	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
–	451	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT	VCCINT
–	452	GNDINT	GND	GND	GND	GND	GND	GND
–	453	VCCIO	VCCIO1	VCCIO1	VCCIO1	VCCIO1	VCCIO1	VCCIO1
1	454	FAST2	181	209	D11	A15	B17	F13
–	455	TDO (6)	180	208	E11	B15	C17	G13
–	456	GNDINT	–	–	GND	–	GND	GND
1	457	I/O	179	207	F11	C15	A16	H13
1	458	I/O, INITDONE (4)	178	206	G13	A16	C16	J15
1	459	I/O, RDYNBSY (2)	177	205	G12	B16	A14	J14
1	460	I/O	–	–	D10	A17	B16	F12
1	461	I/O, CLKUSR (2)	176	204	H12	C16	C15	K14
1	462	I/O	–	203	C10	B17	D16	E12

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	208-Pin PQFP (1)	240-Pin PQFP (1)	484-Pin FineLine BGA	356-Pin BGA	652-Pin BGA	672-Pin FineLine BGA
1	463	I/O	175	202	C9	A18	A15	E11
1	464	I/O	174	201	G11	C17	B15	J13
1	465	I/O, DATA1 (2)	173	200	H11	B18	C13	K13
1	466	I/O	–	–	F10	A19	E16	H12
–	467	GNDIO	GND	GND	GND	GND	GND	GND
–	468	VCCIO	VCCIO1	VCCIO1	–	VCCIO1	VCCIO1	VCCIO1
1	469	I/O	171	198	C8	B19	B14	E10
1	470	I/O	–	197	D9	C18	D15	F11
1	471	I/O	170	196	E10	A20	A13	G12
1	472	I/O, DATA2 (2)	168	195	G10	B20	A8	J12
1	473	I/O	167	–	E9	C19	A12	G11
1	474	I/O	166	194	C7	A21	B13	E9
1	475	I/O	165	193	D7	A22	C14	F9
1	476	I/O	164	192	H10	B21	E15	K12
1	477	I/O	–	–	F9	C20	A11	H11
1	478	I/O	–	191	C6	A23	D14	E8
–	479	VCCIO	VCCIO1	VCCIO1	VCCIO1	VCCIO1	VCCIO1	VCCIO1
1	480	I/O	–	190	D6	A24	B12	F8
1	481	I/O, DATA3 (2)	163	189	D8	B22	B7	F10
1	482	I/O	162	187	C5	B23	A10	E7
1	483	I/O	161	186	E8	C21	E14	G10
1	484	I/O	–	–	F8	B24	B11	H10
1	485	I/O, DATA4 (2)	160	185	E7	A25	B5	G9
1	486	I/O	159	184	G9	C22	C12	J11
1	487	I/O	158	183	D5	C23	D13	F7
1	488	I/O	–	182	C4	B25	E13	E6
1	489	I/O, DATA5 (2)	157	181	D4	C24	E7	F6
–	490	GNDIO	GND	GND	GND	GND	GND	GND

Pin Name	208-Pin PQFP (1)	240-Pin PQFP (1)	356-Pin BGA	484-Pin FineLine BGA	652-Pin BGA	672-Pin FineLine BGA
MSEL0 (6)	25	29	P1	L19	U35	N21
MSEL1 (6)	26	30	P2	L18	W35	N20
nSTATUS (6)	82	92	AF15	W11	AN17	AA13
nCONFIG (6)	29	33	R1	M19	W32	P21
DCLK (6)	132	152	N25	L5	U3	N7
CONF_DONE (6)	83	93	AE15	W10	AM17	AA12
INIT_DONE (4)	178	206	A16	G13	C16	J15
nCE (6)	130	150	P26	M4	U1	P6
nCEO (6)	185	213	A12	E12	C19	G14
nWS (2)	145	164	H22	M7	M1	P9
nRS (2)	142	161	H24	L8	N1	N10
nCS (2)	141	160	J24	K7	P2	M9
CS (2)	138	157	K25	P4	R2	T6
RDYnBSY (2)	177	205	B16	G12	A14	J14
CLKUSR (2)	176	204	C16	H12	C15	K14
DATA7 (2)	146	166	G23	K8	M6	M10
DATA6 (2)	150	169	F24	J6	L6	L8
DATA5 (2)	157	181	C24	D4	E7	F6
DATA4 (2)	160	185	A25	E7	B5	G9
DATA3 (2)	163	189	B22	D8	B7	F10
DATA2 (2)	168	195	B20	G10	A8	J12
DATA1 (2)	173	200	B18	H11	C13	K13
DATA0 (6), (7)	133	153	M26	L4	U4	N6
TDI(6)	129	149	P25	M5	W1	P7
TDO (6)	180	208	B15	E11	C17	G13
TCK (6)	76	87	AE12	W12	AN19	AA14
TMS (6)	75	86	AF11	W13	AM19	AA15
TRST (6)	186	214	B12	D12	D19	F14
Dedicated Fast I/O Pins	77, 81, 181, 184	88, 91, 209, 212	A13, A15, AF12, AE14	D11, F12, V11, V12	B17, B19, AP17, AP19	F13, H14, Y13, Y14
CLK1p	27	31	P3	M18	W34	P20
CLK2p	131	151	N26	L6	U2	N8
CLK3p	31	34	R4	K17	Y34	M19
CLK4p	134	154	M23	N4	T2	R6
LOCK2 (10)	119	138	T24	R4	AB6	U6
LOCK4 (10)	116	135	V25	U5	AC6	W7
CLKLK_ENA (6), (11)	28	32	P4	M14	W33	P16
CLKLK_OUT2p (9)	120	139	R23	P5	Y3	T7
CLKLK_FB2p	135	155	L25	R6	T4	U8
DEV_CLRn (4)	137	156	L23	N7	T6	R9
DEV_OE (4)	124	143	R26	N6	Y5	R8

Pin Name	208-Pin PQFP (1)	240-Pin PQFP (1)	356-Pin BGA	484-Pin FineLine BGA	652-Pin BGA	672-Pin FineLine BGA
VCCINT	36, 23, 11, 3, 1, 182, 156, 154, 148, 126, 121, 109, 105, 79, 52, 48	39, 27, 14, 5, 1, 210, 179, 176, 168, 145, 140, 127, 122, 90, 60, 52	A14, AB25, AB3, AF13, AF14, B14, E23, E1, H1, J23, L1, M25, R2, T22, U4, Y26	B1, B22, H9, J8, J13, K11, K14 L10, M13, M22, N9, N12, P10, P15, R7, R14, AA1, AA22	A17, A19, AA31, AA4, AC3, AC32, AE2, AE33, AG1, AH31, AH35, AH4, AK33, AL12, AL2, AL24, AM12, AM24, AR17, AR19, D12, D24, E12, E24, F3, F35, G30, H1, H5, K31, L3, M30, N35, N4, R34, R5, U34, U5, W3, W31	A3, A24, B3, B8, B19, B24, C1, C2, C25, C26, D3, D24, K11, L10, L15, M13, M16, N2, N12, P15, P24, P25, R11, R14, T12, T17, U9, U16, AC3, AC24, AD1, AD2, AD25, AD26, AE3, AE8, AE19, AE24, AF3, AF24
VCCIO1	172	199	C14, A26,	G8, J10	C4, D5, E17	A6, J10, L12
VCCIO2	208,189	229	A1, C12,	H14, K12	E19, D31, C32	A13, K16, M14
VCCIO3	8	12	M5, C1	J15, L13	F30, F31, U30	A21, L17, N15
VCCIO4	42	45	AD1, P5	L22, N14, R16	W30, AL31, AL32	N24, R16, U18
VCCIO5	80, 53	67	AD12, AF1	P13, T15	AN32, AN33, AL19	T15, V17, AF21
VCCIO6	86	120, 97	AF26, AD14	N11, R9, T8	AL17, AM5, AN4	R13, U11, V10, AF13
VCCIO7	115	148	P22, AD26	M10, P8	AL3, AL4, W6	P12, T10, AF6
VCCIO8	136	177	C26, M22	H7, K9, L1	U6, E3, E4	K9, M11, N3
VCC_CKLK2 (3)	125	144	P23	L9	W4	N11
VCC_CKLK4 (3)	140	159	K24	M8	R4	P10
VCC_CKOUT2 (8)	123	142	R25	T5	Y1	V7

Pin Name	208-Pin PQFP (1)	240-Pin PQFP (1)	356-Pin BGA	484-Pin FineLine BGA	652-Pin BGA	672-Pin FineLine BGA
GND	43, 39, 35, 24, 16, 12, 10, 4, 199, 183, 169, 153, 149, 147, 143, 127, 118, 114, 110, 95, 78, 64, 47	175, 167, 165, 162, 146, 137, 132, 128, 108, 89, 78, 56, 51, 42, 38, 28, 26, 19, 15, 6, 240, 218, 211, 188	AB4, AB5, AC3, AC22, AC23, AC24, AD2, AD13, AD25, AE1, AE13, AE26, B1, B13, B26, C2, C13, C25, D3, D4, D22, D23, D24, E5, N3, N4, N5, N22, N23, N24	A1, A11, A22, B2, B21, F6, F17, G7, G16, H8, H15, J9, J11, J14, K10, K13, L2, L11, L12, M1, M11, M12, M21, N10, N13, P9, P14, R8, R15, T7, T16, U6, U17, AA2, AA21,AB1, AB11, AB22	A1, A18, A35, AK18, AL18, AL30, AL5, AL6, AM18, AM2, AM3, AM31, AM32, AM33, AM34, AM4, AN1, AN18, AN2, AN3, AN34, AN35, AP1, AP18, AP2, AP34, AP35, AR1, AR18, AR35, B1, B18, B2, B34, B35, C18, C2, C3, C33, C34, C35, D17, D18, D2, D3, D32, D33, D34, D4, E18, E30, E31, E32, E33, E5, E6, F18, V1, V2, V3, V30, V31, V32, V33, V34, V4, V5, V6, V35	A2, A8, A14, A19, A25, AC4, AC23, AD3, AD13, AD24, AE1, AE2, AE6, AE21, AE25, AE26, AF2, AF8, AF14, AF19, AF25, B1, B2, B6, B21, B25, B26, C3, C13, C24, D4, D23, H8, H19, J9, J18, K10, K17, L11, L13, L16, M12, M15, N1, N4, N13, N14, N25, N26, P1, P2, P3, P13, P14, P23, P26, R12, R15, T11, T16, U10, U17, V9, V18, W8, W19
GND_CKLK2 (3)	128	147	P24	M9	W2	P11
GND_CKLK4 (3)	139	158	L22	N8	R3	R10
GND_CKOUT2 (8)	122	141	R24	T4	Y2	V6

Pin Name	208-Pin PQFP (1)	240-Pin PQFP (1)	356-Pin BGA	484-Pin FineLine BGA	652-Pin BGA	672-Pin FineLine BGA
No Connect (N.C.)				A9, A10, A12, A13, A14, AB9, AB10, AB12, AB13, AB14	A2, A29, A3, A30, A31, A32, A33, A34, A4, A5, A6, A7, A9, AL10, AL11, AL25, AL26, AL27, AL28, AL29, AL7, AL8, AL9, AM10, AM11, AM25, AM26, AM27, AM28, AM29, AM30, AM6 AM7, AM8, AM9, AN10, AN26, AN27, AN28, AN29, AN30, AN31, AN5, AN6, AN7, AN8, AN9, AP27, AP28, AP29, AP3, AP30, AP31, AP32, AP33, AP4, AP5, AP6, AP7, AP8, AP9, AR2, AR29, AR3, AR30, AR31, AR32, AR33 AR34, AR4, AR5, AR6, AR7, B10, B27, B28, B29, B3, B30, B31, B32, B33, B4, B6, B8, B9, C10, C11, C26, C27, C28, C29, C30, C31, C5, C6, C7, C8, C9, D10, D11, D25, D26, D27, D28, D29, D30, D6, D7, D8, D9, E10, E11, E25, E26, E27, E28, E29, E8, E9	A4, A5, A7, A9, A10, A11, A12, A15, A16, A17, A18, A20,A22, A23, B4, B5, B7, B9, B10, B11, B12, B13, B14, B15, B16, B17, B18, B20, B22, B23, C5, C6, C7, C8, C9, C10, C11, C12, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D20, D21, D22, E23, E24, F23, F24, G23, H23, Y3, Y4, Y23, Y24, AA3, AA4, AA23, AA24, AB3, AB4, AB23, AB24, AC5, AC6, AC7, AC8, AC9, AC10, AC11, AC12, AC13, AC14, AC15, AC16, AC17, AC18, AC19, AC20, AC21, AC22, AD4, AD5, AD6, AD7, AD8, AD9, AD10, AD11, AD12, AD14, AD15, AD16, AD17, AD18, AD19, AD20, AD21, AD22, AD23, AE4, AE5, AE7, AE9, AE10, AE11, AE12, AE13, AE14, AE15, AE16, AE17, AF4, AF5, AF7, AF9, AF10, AF11, AF12, AF15, AF16, AF17
Total User I/O Pins (12)	136	168	271	376	376	376

Notes:

(1) For the 144-pin, 208-pin, and 240-pin PQFP packages, four unique VCCIO levels are supported. The VCCIO pins for I/O banks 1 and 8 must be at the same level. The VCCIO pins for banks 6 and 7 must be at the same level. The VCCIO pins for I/O banks 4 and 5 must be at the same level. The VCCIO pins for I/O banks 2 and 3 must be at the same level. However, unique VREF settings are supported for each of the eight I/O banks.

(2) This pin can be used as a user I/O pin after configuration.

(3) This pin is the power or ground for the ClockLock and ClockBoost circuitry. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device. VCC_CKLK has the same voltage specifications as the VCCINT and should be connected to a 1.8-V power supply. If the ClockLock or ClockBoost circuitry is not used, this power or ground pin should be connected to VCCINT or GNDINT, respectively.

(4) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.

(5) This pin is the complementary signal for the LVDS pair on dedicated inputs and outputs that can be configured for the LVDS standard. If not used for the LVDS pair, these pins are regular I/O pins. Pins with the "n" suffix carry the negative signal for the LVDS channel. Pins with a "p" suffix carry the positive signal for the LVDS channel.

(6) This pin is a dedicated pin; it is not available as a user I/O pin.

(7) This pin is tri-stated in user mode.

(8) This pin is the power or ground for the external output of a PLL. These pins should be set to the VCCIO level/standard desired for the external clock ouput. To ensure noise resistance, the power and ground supply to the PLL external output should be isolated from the power and ground to the rest of the VCCIO and GNDIO pins. If the PLL or external output is not used, this power or ground pin should be connected to VCCIO or GNDIO, respectively.

(9) The CLKLK_OUT pin is powered by the VCC_CKOUT and GND_CKOUT pins.

(10) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry is locked to the incoming clock and generates an internal clock, LOCK is driven high. LOCK remains high if a periodic clock stops clocking. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.

(11) This pin is the active high enable pin for all of the PLL circuits in the device. When de-asserted, all PLLs are reset to their default, unlocked state and will stop clocking. Once re-asserted, the PLLs will lock again and start clocking. If this pin function is not needed, the pin should be connected to VCCINT.

(12) The user I/O pin count includes dedicated inputs and dedicated clock inputs. It does not include the dedicated clock feedback and output pins.

Pin Name (1)	**652-Pin BGA**	**655-Pin PGA**	**672-Pin FineLine BGA**
MSEL0 (2)	U35	A23	N21
MSEL1 (2)	W35	C23	N20
nSTATUS (2)	AN17	AE41	AA13
nCONFIG (2)	W32	C25	P21
DCLK (2)	U3	BA23	N7
CONF_DONE (2)	AM17	AC47	AA12
INIT_DONE (3)	C16	AE7	J15
nCE (2)	U1	BE25	P6
nCEO (2)	C19	AC9	G14
nWS (4)	M1	BF14	P9
nRS (4)	N1	AY20	N10
nCS (4)	P2	BB20	M9
CS (4)	R2	BD20	T6
RDYnBSY (4)	A14	AH4	J14
CLKUSR (4)	C15	AH6	K14
DATA7 (4)	M6	BG13	M10
DATA6 (4)	L6	BB16	L8
DATA5 (4)	E7	BC3	F6
DATA4 (4)	B5	AR7	G9
DATA3 (4)	B7	AV4	F10
DATA2 (4)	A8	AP6	J12
DATA1 (4)	C13	AH8	K13
DATA0 (2), (5)	U4	BE23	N6
TDI (2)	W1	BG23	P7
TDO (2)	C17	AE1	G13
TCK (2)	AN19	AC45	AA14
TMS (2)	AM19	AD40	AA15
TRST (2)	D19	AD2	F14
Dedicated Inputs	B17, B19, AP17, AP19	AB4, AC5, AC43, AE43	F13, H14, Y13, Y14
Dedicated Clock Pins	U2, W34	H24, AY24	N8, P20
LOCK (6)	AB6	BG29	U6
CLK2 (7)	U2	AY24	N8
DEV_CLRn (3)	T6	AY22	R9
DEV_OE (3)	Y5	BF26	R8
VCCINT	A17, A19, D12, D24, E12, E24, F3, F35, G30, H1, H5, K31, L3, M30, N4, N35 R5, R34, U5, U34, W3, W31, W33, AA4, AA31, AC3, AC32, AE2, AE33, AG1, AH4, AH31, AH35, AK33, AL2, AL12, AL24, AM12, AM24, AR17, AR19	A3, A45, B24, C1, C11, C19, C29, C37, C47, D24, G47, L3, L45, N1, N47, W3, W45, AA1, AA47, AD4, AD44, AG1, AG47, AJ3, AJ45, AR1, AR47, AU3, AU45, AY8, BA1, BA47, BD24, BE1, BE11, BE19, BE29, BE37, BE47, BG3, BG45	A3, A24, B3, B8, B19, B24, C1, C2, C25, C26, D3, D24, K11, L10, L15, M13, M16, N2, N12, P15, P16, P24, P25, R11, R14, T12, T17, U9, U16, AC3, AC24, AD1, AD2, AD25, AD26, AE3, AE8, AE19, AE24, AF3, AF24
VCCIO	AL3, AL4, AL17, AL19, AL31, AL32, AM5, AN4, AN32, AN33, C4, C32, D5, D31, E3, E4, E17, E19, F30, F31, U6, U30, W6, W30,	E9, E15, E21, E27, E33, E39, G7, G41, J5, J43, R5, R43, AA5, AA43, AG5, AG43, AN5, AN43, AW5, AW43, BA7, BA41, BC9, BC15, BC21, BC27, BC33, BC39	A6, A13, A21, J10, K9, K16, L12, L17, M11, M14, N3, N15, N24, P12, R13, R16, T10, T15, U11, U18, V10, V17, AF6, AF13, AF21
VCC_CKLK (8)	W4	BD28	N11

Pin Name (1)	**652-Pin BGA**	**655-Pin PGA**	**672-Pin FineLine BGA**
GNDINT	A1, A18, A35, B1, B2, B18, B34, B35, C2, C3, C18, C33, C34, C35, D2, D3, D4, D17, D18, D32, D33, D34, E5, E6, E18, E30, E31, E32, E33, F18, V1, V2, V3, V4, V5, V6, V30, V31, V32, V33, V34, V35, AK18, AL5, AL6, AL18, AL30, AM18, AM2, AM3, AM4, AM31, AM32, AM33, AM34, AN1, AN2, AN3, AN18, AN34, AN35, AP1, AP2, AP18, AP34, AP35, AR1, AR18, AR35,	A47, B2, C13, C21, C27, C35, C45, D4, F24, J1, J47, N3, N45, R1, R47, W1, W47, AA3, AA45, AD6, AD8, AD42, AG3, AG45, AJ1, AJ47, AN1, AN47, AR3, AR45, AW1, AW47, BB24, BE3, BE13, BE21, BE27, BE35, BE45, BG1, BG47	A2, A8, A14, A19, A25, B1, B2, B6, B21, B25, B26, C3, C13, C24, D4, D23, H8, H19, J9, J18, K10, K17, L11, L13, L16, M12, M15, N1, N4, N13, N14, N25, N26, P1, P2, P3, P13, P14, P23, P26, R12, R15, T11, T16, U10, U17, V9, V18, W8, W19, AC4, AC23, AD3, AD13, AD24, AE1, AE2, AE6, AE21, AE25, AE26, AF2, AF8, AF14, AF19, AF25
GNDIO (9)	–	E7, E13, E19, E29, E35, E41, G5, G43, H40, N5, N43, W5, W43, AJ5, AJ43, AR5, AR43, AY40, BA5, BA43, BC7, BC13, BC19, BC29, BC35, BC41, BF46	–
GND_CKLK (8)	W2	BD26	P11
No Connect (N.C.)	–	–	A15, A16, B13, B14, B15, B16, C11, C12, C14, C15, C16, AD11, AD12, AD14, AD15, AD16, AE12, AE13, AE14, AE15, AF12, AF15,
Total User I/O Pins (10)	502	502	502

Notes:

(1) All pins that are not listed are user I/O pins.
(2) This pin is a dedicated pin; it is not available as a user I/O pin.
(3) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.
(4) This pin can be used as a user I/O pin after configuration.
(5) This pin is tri-stated in user mode.
(6) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry is locked to the incoming clock and generates an internal clock, LOCK is driven high. LOCK remains high if a periodic clock stops clocking. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.
(7) This pin drives the ClockLock and ClockBoost circuitry.
(8) This pin is the power or ground for the ClockLock and ClockBoost circuitry. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device. VCC_CKLK has the same voltage specifications as the VCCINT and should be connected to a 2.5-V power supply. If the ClockLock or ClockBoost circuitry is not used, this power or ground pin should be connected to VCCINT or GNDINT, respectively.
(9) GNDIO and GNDINT are connected together in BGA packages.
(10) The user I/O pin count includes dedicated inputs, dedicated clock inputs, and all I/O pins.

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
8	1	I/O	F6	E5
8	2	I/O	F5	E3
8	3	I/O	F4	F5
8	4	I/O	C1	F4
–	5	VCCINT	VCCINT	VCCINT
–	6	GNDINT	GND	GND
8	7	I/O	D1	E4
8	8	I/O	E2	F3
8	9	I/O	G6	D5
8	10	I/O	G5	G5
8	11	I/O	G4	G3
–	12	VCCIO	VCCIO8	VCCIO8
8	13	I/O	G3	G8
8	14	I/O	F2	G4
8	15	I/O	E1	C4
8	16	I/O	G2	G6
8	17	I/O	H6	H5
–	18	VCCINT	VCCINT	VCCINT
–	19	GNDINT	GND	GND
8	20	I/O	H4	G7
8	21	I/O	H3	H7
8	22	I/O	F1	H4
8	23	I/O	H2	H6
8	24	I/O	G1	K7
–	25	GNDIO	GND	GND
8	26	I/O	J6	J5
8	27	I/O	J5	H9
8	28	I/O	J4	J8
8	29	I/O	J3	H3
8	30	I/O	J2	K3
–	31	VCCINT	VCCINT	VCCINT
–	32	GNDINT	GND	GND
8	33	I/O	J1	J4
8	34	I/O	K6	K5
8	35	I/O	K5	J6
8	36	I/O	K4	L6
8	37	I/O	K3	J7
–	38	VCCIO	VCCIO8	VCCIO8
8	39	I/O	K2	J3
8	40	I/O	K1	K8
8	41	I/O, DATA6 (1)	L6	L8
8	42	I/O	L5	K6
8	43	I/O	L4	K4
–	44	VCCINT	VCCINT	VCCINT
–	45	GNDINT	GND	GND
8	46	I/O	L2	N5
8	47	I/O	L1	M8
8	48	I/O, DATA7 (1)	M6	M10

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
8	49	I/O	M5	M6
8	50	I/O	M4	L7
–	51	GNDIO	GND	GND
8	52	I/O	M3	L9
8	53	I/O	M2	M7
8	54	I/O, nWS (1)	M1	P9
8	55	I/O	N6	L5
8	56	I/O	N5	P8
–	57	VCCINT	VCCINT	VCCINT
–	58	GNDINT	GND	GND
8	59	I/O	N3	L4
8	60	I/O	N2	L3
8	61	I/O, nRS (1)	N1	N10
8	62	I/O	P6	R4
8	63	I/O	P5	M5
–	64	VCCIO	VCCIO8	VCCIO8
8	65	I/O	P4	M3
8	66	I/O	P3	P4
8	67	I/O, nCS (1)	P2	M9
8	68	I/O	P1	R3
8	69	I/O	R6	P5
–	70	VCCINT	VCCINT	VCCINT
–	71	GNDINT	GND	GND
–	72	VCC_CKLK4 (2)	R4	P10
–	73	GND_CKLK4 (2)	R3	R10
–	74	GND_CKLK4 (2)	R3	R10
8	75	I/O, CS (1)	R2	T6
8	76	I/O	R1	M4
8	77	I/O, DEV_CLRn (3)	T6	R9
–	78	VCCIO	VCCIO8	–
–	79	GNDIO	GND	GND
8	80	I/O, CLKLK_FB2n (4)	T5	T8
8	81	CLKLK_FB2p	T4	U8
8	82	I/O, CLK4n (4)	T3	R7
8	83	CLK4p	T2	R6
8	84	I/O, CLK2n (4)	T1	N9
–	85	VCCINT	VCCINT	VCCINT
–	86	GNDINT	GND	GND
–	87	DATA0 (5), (6)	U4	N6
–	88	DCLK (5)	U3	N7
8	89	CLK2p	U2	N8
–	90	nCE (5)	U1	P6
–	91	TDI (5)	W1	P7
–	92	VCCIO	VCCIO7	VCCIO7
–	93	GND_CKLK2 (2)	W2	P11
–	94	GND_CKLK2 (2)	W2	P11
–	95	GNDINT	GND	GND
–	96	VCCINT	VCCINT	VCCINT

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
–	97	VCC_CKLK2 (2)	W4	N11
7	98	I/O, DEV_OE (3)	Y5	R8
–	99	VCC_CKOUT2 (7)	Y1	V7
–	100	GND_CKOUT2 (7)	Y2	V6
–	101	CLKLK_OUT2p (8)	Y3	T7
7	102	I/O, CLKLK_OUT2n (4)	Y4	U7
–	103	VCCIO	VCCIO7	VCCIO7
7	104	I/O, LVDSTXINCLK1p	W5	D1
7	105	I/O, LVDSTXINCLK1n (4)	Y6	D2
7	106	I/O, LOCK2 (9)	AB6	U6
7	107	I/O, LVDSTXOUTCLK1n (4)	AA2	E1
7	108	I/O, LVDSTXOUTCLK1p	AA3	E2
–	109	GNDINT	GND	GND
–	110	VCCINT	VCCINT	VCCINT
7	111	I/O, LVDSTX01p	AA5	F1
7	112	I/O, LVDSTX01n (4)	AA6	F2
7	113	I/O	AB1	R5
7	114	I/O, LVDSTX02n (4)	AB2	G1
7	115	I/O, LVDSTX02p	AB3	G2
–	116	GNDIO	GND	GND
7	117	I/O, LVDSTX03p	AB4	H1
7	118	I/O, LVDSTX03n (4)	AB5	H2
7	119	I/O	AA1	T5
7	120	I/O, LVDSTX04n (4)	AC1	J1
7	121	I/O, LVDSTX04p	AC2	J2
–	122	GNDINT	GND	GND
–	123	VCCINT	VCCINT	VCCINT
7	124	I/O, LVDSTX05p	AC4	K1
7	125	I/O, LVDSTX05n (4)	AC5	K2
7	126	I/O, LOCK4 (9)	AC6	W7
7	127	I/O, LVDSTX06n (4)	AD1	L1
7	128	I/O, LVDSTX06p	AD2	L2
–	129	VCCIO	VCCIO7	VCCIO7
7	130	I/O, LVDSTX07p	AD3	M1
7	131	I/O, LVDSTX07n (4)	AD4	M2
7	132	I/O	AD5	T3
7	133	I/O, LVDSTX08n (4)	AD6	R1
7	134	I/O, LVDSTX08p	AE1	R2
–	135	GNDINT	GND	GND
–	136	VCCINT	VCCINT	VCCINT
7	137	I/O, LVDSTX09p	AE3	T1
7	138	I/O, LVDSTX09n (4)	AE4	T2
7	139	I/O	AE5	U5

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
7	140	I/O, LVDSTX10n (4)	AE6	U1
7	141	I/O, LVDSTX10p	AF1	U2
–	142	GNDIO	GND	GND
7	143	I/O, LVDSTX11p	AF2	V1
7	144	I/O, LVDSTX11n (4)	AF3	V2
7	145	I/O	AF4	T4
7	146	I/O, LVDSTX12n (4)	AF5	W1
7	147	I/O, LVDSTX12p	AF6	W2
–	148	GNDINT	GND	GND
–	149	VCCINT	VCCINT	VCCINT
7	150	I/O, LVDSTX13p	AH1	Y1
7	151	I/O, LVDSTX13n (4)	AG2	Y2
7	152	I/O	AG3	U4
7	153	I/O, LVDSTX14n (4)	AG4	AA1
7	154	I/O, LVDSTX14p	AG5	AA2
–	155	VCCIO	VCCIO7	VCCIO7
7	156	I/O, LVDSTX15p	AG6	AB1
7	157	I/O, LVDSTX15n (4)	AJ1	AB2
7	158	I/O	AH2	W4
7	159	I/O, LVDSTX16n (4)	AK1	AC1
7	160	I/O, LVDSTX16p	AH3	AC2
–	161	GNDINT	GND	GND
–	162	VCCINT	VCCINT	VCCINT
7	163	I/O	AH5	U3
7	164	I/O	AH6	V3
7	165	I/O	AJ2	W5
7	166	I/O	AL1	W6
7	167	I/O	AK2	V5
–	168	GNDIO	GND	GND
7	169	I/O	AJ3	V4
7	170	I/O	AJ4	W3
7	171	I/O	AJ5	Y5
7	172	I/O	AJ6	AB5
7	173	I/O	AM1	AA5
–	174	GNDINT	GND	GND
–	175	VCCINT	VCCINT	VCCINT
7	176	I/O	AK3	Y6
7	177	I/O	AK4	AA6
7	178	I/O	AK5	AA7
7	179	I/O	AK6	AB6
–	180	VCCIO	VCCIO7	VCCIO7
–	181	VCCIO	VCCIO6	VCCIO6
6	182	I/O	AL7	AB4
6	183	I/O	AM6	AA4
6	184	I/O	AP3	AC5
6	185	I/O	AN5	Y4
6	186	I/O	AR2	AE4
6	187	I/O	AP4	AB3

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
6	188	I/O	AL8	AF4
6	189	I/O	AM7	Y3
6	190	I/O	AN6	AD4
6	191	I/O	AR3	AA3
–	192	GNDIO	GND	GND
6	193	I/O	AP5	AE5
6	194	I/O	AL9	AD5
6	195	I/O	AR4	AD6
6	196	I/O	AM8	AB7
6	197	I/O	AN7	Y7
6	198	I/O	AP6	AC6
6	199	I/O	AR5	AB8
6	200	I/O	AM9	AF5
6	201	I/O	AL10	V8
6	202	I/O	AN8	AC7
–	203	VCCIO	VCCIO6	VCCIO6
6	204	I/O	AP7	AD7
6	205	I/O	AR6	T9
6	206	I/O	AM10	AE7
6	207	I/O	AN9	AA9
6	208	I/O	AL11	AF7
6	209	I/O	AP8	AA8
6	210	I/O	AR7	AC8
6	211	I/O	AM11	Y8
6	212	I/O	AN10	AD8
6	213	I/O	AP9	Y9
–	214	GNDIO	GND	GND
–	215	VCCINT	VCCINT	VCCINT
–	216	VCCINT	VCCINT	VCCINT
–	217	GNDINT	GND	GND
–	218	GNDINT	GND	GND
6	219	I/O	AR8	W9
6	220	I/O	AN11	AB9
6	221	I/O	AP10	W10
6	222	I/O	AR9	AC9
6	223	I/O	AL13	Y10
6	224	I/O	AM13	AD9
6	225	I/O	AN12	AA10
6	226	I/O	AP11	AB11
6	227	I/O	AL14	V11
6	228	I/O	AR10	AB10
–	229	VCCIO	VCCIO6	VCCIO6
6	230	I/O	AN13	AC10
6	231	I/O	AP12	AA11
6	232	I/O	AM14	AE9
6	233	I/O	AR11	Y11
6	234	I/O	AL15	AF9
6	235	I/O	AN14	W11

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
6	236	I/O	AP13	AF11
6	237	I/O	AR12	V12
6	238	I/O	AR13	AE10
6	239	I/O	AM15	W12
–	240	GNDIO	GND	GND
6	241	I/O	AN15	Y12
6	242	I/O	AL16	T13
–	243	VCCIO	VCCIO6	VCCIO6
6	244	I/O	AP14	W14
6	245	I/O	AR14	AB12
6	246	I/O	AP15	AF10
6	247	I/O	AR15	U13
6	248	I/O, LVDSDESKEW	AM16	U12
6	249	I/O	AN16	W13
6	250	I/O	AP16	AE11
6	251	I/O	AR16	V13
–	252	CONF_DONE (5)	AM17	AA12
–	253	nSTATUS (5)	AN17	AA13
5	254	FAST4	AP17	Y13
–	255	VCCIO	VCCIO5	VCCIO5
–	256	VCCINT	VCCINT	VCCINT
–	257	VCCINT	VCCINT	VCCINT
–	258	GNDINT	GND	GND
–	259	GNDINT	GND	GND
5	260	FAST3	AP19	Y14
–	261	TCK (5)	AN19	AA14
–	262	TMS (5)	AM19	AA15
5	263	I/O	AR20	AC13
5	264	I/O	AP20	AD17
5	265	I/O	AN20	AC12
5	266	I/O	AM20	AC14
5	267	I/O	AR21	AD10
5	268	I/O	AP21	AB13
5	269	I/O	AR22	V14
5	270	I/O	AP22	AB14
5	271	I/O	AL20	Y15
5	272	I/O	AN21	AC11
–	273	GNDIO	GND	GND
5	274	I/O	AM21	AD18
5	275	I/O	AR23	U14
5	276	I/O	AR24	AC15
5	277	I/O	AP23	V15
5	278	I/O	AN22	AB15
5	279	I/O	AL21	W15
5	280	I/O	AR25	AB16
5	281	I/O	AM22	T14
5	282	I/O	AP24	AD19
5	283	I/O	AN23	AA16

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
–	284	VCCIO	VCCIO5	VCCIO5
5	285	I/O	AR26	Y16
5	286	I/O	AL22	AC16
5	287	I/O	AP25	W16
5	288	I/O	AN24	AC17
5	289	I/O	AM23	U15
5	290	I/O	AL23	AB17
5	291	I/O	AR27	V16
5	292	I/O	AP26	AE16
5	293	I/O	AN25	AA17
5	294	I/O	AR28	AD20
–	295	VCCINT	VCCINT	VCCINT
–	296	VCCINT	VCCINT	VCCINT
–	297	GNDINT	GND	GND
–	298	GNDINT	GND	GND
–	299	GNDIO	GND	GND
5	300	I/O	AP27	AB18
5	301	I/O	AN26	Y17
5	302	I/O	AM25	AF16
5	303	I/O	AR29	AA18
5	304	I/O	AP28	AC18
5	305	I/O	AL25	W17
5	306	I/O	AN27	AE17
5	307	I/O	AM26	Y18
5	308	I/O	AR30	AF17
5	309	I/O	AP29	W18
–	310	VCCIO	VCCIO5	VCCIO5
5	311	I/O	AN28	AA19
5	312	I/O	AL26	AD21
5	313	I/O	AM27	Y19
5	314	I/O	AR31	AD22
5	315	I/O	AP30	W20
5	316	I/O	AN29	AC19
5	317	I/O	AM28	Y20
5	318	I/O	AR32	AB20
5	319	I/O	AL27	AB19
5	320	I/O	AP31	AC20
–	321	GNDIO	GND	GND
5	322	I/O	AR33	AD23
5	323	I/O	AN30	AA20
5	324	I/O	AM29	AB24
5	325	I/O	AL28	AC22
5	326	I/O	AP32	AC21
5	327	I/O	AR34	Y23
5	328	I/O	AN31	Y24
5	329	I/O	AP33	AA23
5	330	I/O	AM30	AA24
5	331	I/O	AL29	AB23

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
–	332	VCCIO	VCCIO5	VCCIO5
–	333	VCCIO	VCCIO4	VCCIO4
4	334	I/O	AL33	AA21
4	335	I/O	AK30	Y22
4	336	I/O	AK31	AB21
4	337	I/O	AK32	U19
–	338	VCCINT	VCCINT	VCCINT
–	339	GNDINT	GND	GND
4	340	I/O	AL34	AB22
4	341	I/O	AM35	V19
4	342	I/O	AJ30	T18
4	343	I/O	AJ31	W21
4	344	I/O	AJ32	V20
–	345	GNDIO	GND	GND
4	346	I/O	AJ33	V21
4	347	I/O	AK34	Y21
4	348	I/O	AL35	W22
4	349	I/O	AJ34	AA22
4	350	I/O	AH30	U20
–	351	VCCINT	VCCINT	VCCINT
–	352	GNDINT	GND	GND
4	353	I/O	AH32	R17
4	354	I/O	AH33	W23
4	355	I/O	AK35	T19
4	356	I/O	AH34	U21
4	357	I/O	AJ35	P17
–	358	VCCIO	VCCIO4	VCCIO4
4	359	I/O	AG30	R18
4	360	I/O	AG31	W24
4	361	I/O	AG32	T20
4	362	I/O	AG33	V24
4	363	I/O	AG34	N16
–	364	VCCINT	VCCINT	VCCINT
–	365	GNDINT	GND	GND
4	366	I/O	AG35	V22
4	367	I/O	AF30	R19
4	368	I/O	AF31	V23
4	369	I/O	AF32	P18
4	370	I/O	AF33	N17
–	371	GNDIO	GND	GND
4	372	I/O	AF34	T21
4	373	I/O	AF35	R21
4	374	I/O	AE30	U22
4	375	I/O	AE31	R20
4	376	I/O	AE32	P22
–	377	VCCINT	VCCINT	VCCINT
–	378	GNDINT	GND	GND
4	379	I/O	AE34	N18

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
4	380	I/O	AE35	U23
4	381	I/O	AD30	N19
4	382	I/O	AD31	N22
4	383	I/O	AD32	L20
–	384	VCCIO	VCCIO4	VCCIO4
4	385	I/O	AD33	M17
4	386	I/O	AD34	T22
4	387	I/O	AD35	M18
4	388	I/O	AC30	T23
4	389	I/O	AC31	R23
–	390	VCCINT	VCCINT	VCCINT
–	391	GNDINT	GND	GND
4	392	I/O	AC33	U24
4	393	I/O	AC34	R24
4	394	I/O	AC35	T24
4	395	I/O	AB30	M21
4	396	I/O	AB31	M24
–	397	GNDIO	GND	GND
4	398	I/O	AB32	M22
4	399	I/O	AB33	R22
4	400	I/O	AB34	M23
4	401	I/O	AB35	L22
4	402	I/O, LOCK1 (9)	AA30	L21
–	403	VCCINT	VCCINT	VCCINT
–	404	GNDINT	GND	GND
4	405	I/O	AA32	L23
4	406	I/O	AA33	L24
4	407	I/O	AA34	N23
–	408	VCC_CKLK1 (2)	AA35	AF18
–	409	GND_CKLK1 (2)	Y30	AE18
–	410	GND_CKLK1 (2)	Y30	AE18
–	411	VCCIO	VCCIO4	VCCIO4
4	412	I/O, CLKLK_FB1n (4)	Y31	AF20
4	413	CLKLK_FB1p	Y32	AE20
4	414	I/O, CLK3n (4)	Y33	M20
4	415	CLK3p	Y34	M19
4	416	I/O, CLK1n (4)	Y35	P19
–	417	VCCINT	VCCINT	VCCINT
–	418	GNDINT	GND	GND
–	419	VCCIO	VCCIO4	VCCIO4
–	420	nCONFIG (5)	W32	P21
–	421	CLKLK_ENA (5), (10)	W33	P16
4	422	CLK1p	W34	P20
–	423	MSEL1 (5)	W35	N20
–	424	MSEL0 (5)	U35	N21
–	425	GNDINT	GND	GND
–	426	VCCINT	VCCINT	VCCINT
–	427	VCC_CKOUT1 (7)	U33	AF22

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
–	428	GND_CKOUT1 (7)	U32	AE22
–	429	CLKLK_OUT1p (8)	U31	AE23
3	430	I/O, CLKLK_OUT1n (4)	T35	AF23
–	431	VCC_CKLK3 (2)	T34	AC26
–	432	GNDIO	GND	GND
–	433	GND_CKLK3 (2)	V35	N25
–	434	GND_CKLK3 (2)	T33	AC25
3	435	I/O, LVDSRXINCLK1p	T32	AB25
3	436	I/O, LVDSRXINCLK1n (4)	T31	AB26
3	437	I/O	T30	J23
3	438	I/O	R35	L19
–	439	GNDINT	GND	GND
–	440	VCCINT	VCCINT	VCCINT
3	441	I/O, LVDSRX01p	R33	AA25
3	442	I/O, LVDSRX01n (4)	R32	AA26
3	443	I/O, LOCK3 (9)	R31	L18
3	444	I/O, LVDSRX02n (4)	R30	Y25
3	445	I/O, LVDSRX02p	P35	Y26
–	446	VCCIO	VCCIO3	VCCIO3
3	447	I/O, LVDSRX03p	P34	W25
3	448	I/O, LVDSRX03n (4)	P33	W26
3	449	I/O	P32	J24
3	450	I/O, LVDSRX04n (4)	P31	V25
3	451	I/O, LVDSRX04p	P30	V26
–	452	GNDINT	GND	GND
–	453	VCCINT	VCCINT	VCCINT
3	454	I/O, LVDSRX05p	N34	U25
3	455	I/O, LVDSRX05n (4)	N33	U26
3	456	I/O	N32	K21
3	457	I/O, LVDSRX06n (4)	N31	T25
3	458	I/O, LVDSRX06p	N30	T26
–	459	GNDIO	GND	GND
3	460	I/O, LVDSRX07p	M35	R25
3	461	I/O, LVDSRX07n (4)	M34	R26
3	462	I/O	M33	K23
3	463	I/O, LVDSRX08n (4)	M32	M25
3	464	I/O, LVDSRX08p	M31	M26
–	465	GNDINT	GND	GND
–	466	VCCINT	VCCINT	VCCINT
3	467	I/O, LVDSRX09p	L35	L25
3	468	I/O, LVDSRX09n (4)	L34	L26
3	469	I/O	L33	K20
3	470	I/O, LVDSRX10n (4)	L32	K25
3	471	I/O, LVDSRX10p	L31	K26
–	472	VCCIO	VCCIO3	VCCIO3
3	473	I/O, LVDSRX11p	L30	J25

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
3	474	I/O, LVDSRX11n (4)	K35	J26
3	475	I/O	K34	K22
3	476	I/O, LVDSRX12n (4)	K33	H25
3	477	I/O, LVDSRX12p	K32	H26
–	478	GNDINT	GND	GND
–	479	VCCINT	VCCINT	VCCINT
3	480	I/O, LVDSRX13p	K30	G25
3	481	I/O, LVDSRX13n (4)	J35	G26
3	482	I/O	H35	K24
3	483	I/O, LVDSRX14n (4)	J34	F25
3	484	I/O, LVDSRX14p	J33	F26
–	485	GNDIO	GND	GND
3	486	I/O, LVDSRX15p	J32	E25
3	487	I/O, LVDSRX15n (4)	J31	E26
3	488	I/O	J30	H24
3	489	I/O, LVDSRX16n (4)	G35	D25
3	490	I/O, LVDSRX16p	H34	D26
–	491	GNDINT	GND	GND
–	492	VCCINT	VCCINT	VCCINT
3	493	I/O	H33	K19
3	494	I/O	H32	J20
3	495	I/O	H31	G22
3	496	I/O	H30	H20
3	497	I/O	G34	H22
–	498	VCCIO	VCCIO3	VCCIO3
3	499	I/O	E35	J22
3	500	I/O	F34	G24
3	501	I/O	G33	H21
3	502	I/O	G32	G21
3	503	I/O	G31	J21
–	504	GNDINT	GND	GND
–	505	VCCINT	VCCINT	VCCINT
3	506	I/O	D35	F22
3	507	I/O	E34	G20
3	508	I/O	F33	F21
3	509	I/O	F32	E22
–	510	VCCIO	VCCIO2	–
–	511	GNDIO	GND	GND
2	512	I/O	E29	E23
2	513	I/O	D30	D22
2	514	I/O	B33	F24
2	515	I/O	C31	E24
2	516	I/O	A34	H23
2	517	I/O	B32	C23
2	518	I/O	E28	G23
2	519	I/O	D29	C22
2	520	I/O	C30	F23
2	521	I/O	A33	B23

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
–	522	VCCIO	VCCIO2	VCCIO2
2	523	I/O	B31	A23
2	524	I/O	E27	E21
2	525	I/O	A32	B22
2	526	I/O	D28	F20
2	527	I/O	C29	D21
2	528	I/O	B30	C21
2	529	I/O	A31	E20
2	530	I/O	D27	J19
2	531	I/O	E26	A22
2	532	I/O	C28	G19
–	533	GNDIO	GND	GND
2	534	I/O	B29	F19
2	535	I/O	A30	E19
2	536	I/O	D26	K18
2	537	I/O	C27	D20
2	538	I/O	E25	H18
2	539	I/O	B28	C20
2	540	I/O	A29	G18
2	541	I/O	D25	D19
2	542	I/O	C26	E18
2	543	I/O	B27	B20
–	544	VCCIO	VCCIO2	VCCIO2
–	545	GNDINT	GND	GND
–	546	GNDINT	GND	GND
–	547	VCCINT	VCCINT	VCCINT
–	548	VCCINT	VCCINT	VCCINT
–	549	GNDINT	–	–
2	550	I/O	A28	A20
2	551	I/O	C25	F18
2	552	I/O	B26	C19
2	553	I/O	A27	E17
2	554	I/O	E23	D18
2	555	I/O	D23	F17
2	556	I/O	C24	C18
2	557	I/O	B25	G17
2	558	I/O	E22	B18
2	559	I/O	A26	H17
–	560	GNDIO	GND	GND
2	561	I/O	C23	F16
2	562	I/O	B24	D17
2	563	I/O	D22	J17
2	564	I/O	A25	E16
2	565	I/O	E21	G16
2	566	I/O	C22	A18
2	567	I/O	B23	H16
2	568	I/O	A24	C17
2	569	I/O	A23	E15

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
2	570	I/O	D21	D16
–	571	VCCIO	VCCIO2	VCCIO2
2	572	I/O	C21	B17
2	573	I/O	E20	F15
2	574	I/O	B22	A17
2	575	I/O	A22	E14
2	576	I/O	B21	H15
2	577	I/O	A21	E13
2	578	I/O	D20	L14
2	579	I/O	C20	G15
2	580	I/O	B20	K15
2	581	I/O	A20	J16
–	582	TRST (5)	D19	F14
–	583	nCEO (5)	C19	G14
1	584	FAST1	B19	H14
–	585	GNDINT	GND	GND
–	586	GNDINT	GND	GND
–	587	VCCINT	VCCINT	VCCINT
–	588	VCCINT	VCCINT	VCCINT
–	589	GNDIO	GND	GND
1	590	FAST2	B17	F13
–	591	TDO (5)	C17	G13
–	592	GNDINT	GND	GND
1	593	I/O	A16	D15
1	594	I/O	B16	D14
1	595	I/O, INITDONE (3)	C16	J15
1	596	I/O	D16	A12
1	597	I/O	A15	D13
1	598	I/O	B15	B11
1	599	I/O, RDYnBSY (1)	A14	J14
1	600	I/O	B14	B12
1	601	I/O	E16	H13
1	602	I/O, CLKUSR (1)	C15	K14
–	603	VCCIO	VCCIO1	VCCIO1
1	604	I/O	D15	F12
1	605	I/O	A13	A11
1	606	I/O	A12	E12
1	607	I/O	B13	A10
1	608	I/O	C14	D12
1	609	I/O	E15	D11
1	610	I/O	A11	E11
1	611	I/O	D14	B10
1	612	I/O	B12	C10
1	613	I/O, DATA1 (1)	C13	K13
–	614	GNDIO	GND	GND
1	615	I/O	A10	J13
1	616	I/O	E14	D10
–	617	VCCIO	VCCIO1	VCCIO1

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA
1	618	I/O	B11	H12
1	619	I/O	C12	E10
1	620	I/O	D13	F11
1	621	I/O	E13	B9
1	622	I/O	A9	G12
1	623	I/O	B10	C9
1	624	I/O	C11	G11
1	625	I/O, DATA2 (1)	A8	J12
–	626	GNDINT	GND	GND
–	627	GNDINT	GND	GND
–	628	VCCINT	VCCINT	VCCINT
–	629	VCCINT	VCCINT	VCCINT
–	630	VCCIO	VCCIO1	VCCIO1
1	631	I/O	B9	E9
1	632	I/O	C10	F9
1	633	I/O	D11	D9
1	634	I/O	A7	K12
1	635	I/O	B8	A9
1	636	I/O	E11	H11
1	637	I/O	C9	D8
1	638	I/O	D10	E8
1	639	I/O	A6	C8
1	640	I/O, DATA3 (1)	B7	F10
–	641	GNDIO	GND	GND
1	642	I/O	C8	F8
1	643	I/O	E10	E7
1	644	I/O	D9	G10
1	645	I/O	A5	C7
1	646	I/O	B6	H10
1	647	I/O	C7	B7
1	648	I/O	D8	J11
1	649	I/O	A4	D7
1	650	I/O	E9	D6
1	651	I/O, DATA4 (1)	B5	G9
–	652	VCCIO	VCCIO1	VCCIO1
1	653	I/O	A3	A7
1	654	I/O	C6	F7
1	655	I/O	D7	E6
1	656	I/O	E8	C5
1	657	I/O	B4	C6
1	658	I/O	A2	B5
1	659	I/O	C5	A5
1	660	I/O	B3	B4
1	661	I/O	D6	A4
1	662	I/O, DATA5 (1)	E7	F6
–	663	GNDIO	GND	GND
–	664	–	–	–

Pin Name	652-Pin BGA	672-Pin FineLine BGA
MSEL0 (5)	U35	N21
MSEL1 (5)	W35	N20
nSTATUS (5)	AN17	AA13
nCONFIG (5)	W32	P21
DCLK (5)	U3	N7
CONF_DONE (5)	AM17	AA12
INIT_DONE (3)	C16	J15
nCE (5)	U1	P6
nCEO (5)	C19	G14
nWS (1)	M1	P9
nRS (1)	N1	N10
nCS (1)	P2	M9
CS (1)	R2	T6
RDYnBSY (1)	A14	J14
CLKUSR (1)	C15	K14
DATA7 (1)	M6	M10
DATA6 (1)	L6	L8
DATA5 (1)	E7	F6
DATA4 (1)	B5	G9
DATA3 (1)	B7	F10
DATA2 (1)	A8	J12
DATA1 (1)	C13	K13
DATA0 (5), (6)	U4	N6
TDI (5)	W1	P7
TDO (5)	C17	G13
TCK (5)	AN19	AA14
TMS (5)	AM19	AA15
TRST (5)	D19	F14
Dedicated Fast I/Os	AP19, AP17, B17, B19	Y14, Y13, F13, H14
CLK1p	W34	P20
CLK2p	U2	N8
CLK3p	Y34	M19
CLK4p	T2	R6
LOCK1 (9)	AA30	L21
LOCK2 (9)	AB6	U6
LOCK3 (9)	R31	L18
LOCK4 (9)	AC6	W7
CLKLK_ENA (5), (10)	W33	P16
CLKLK_OUT1p (8)	U31	AE23
CLKLK_OUT2p (8)	Y3	T7
CLKLK_FB1p	Y32	AE20
CLKLK_FB2p	T4	U8
DEV_CLRn (3)	T6	R9
DEV_OE (3)	Y5	R8

Pin Name	652-Pin BGA	672-Pin FineLine BGA
VCCINT	A17, A19, AA31, AA4, AC3, AC32, AE2, AE33, AG1, AH31, AH35, AH4, AK33, AL12, AL2, AL24, AM12, AM24, AR17, AR19, D12, D24, E12, E24, F3, F35, G30, H1, H5, K31, L3, M30, N35, N4, R34, R5, U34, U5, W3, W31	A3, A24, B3, B8, B19, B24,C1, C2, C25, C26, D3, D24,K11, L10, L15, M13, M16, N2, N12, P15, P24, P25, R11, R14, T12, T17, U9, U16, AC3, AC24, AD1, AD2, AD25,AD26, AE3, AE8, AE19, AE24, AF3, AF24
VCCIO1	C4, D5, E17	A6, J10, L12
VCCIO2	E19, D31, C32	A13, K16, M14
VCCIO3	F30, F31, U30	A21, L17, N15
VCCIO4	W30, AL31, AL32	N24, R16, U18
VCCIO5	AN32, AN33, AL19	T15, V17, AF21
VCCIO6	AL17, AM5, AN4	R13, U11, V10, AF13
VCCIO7	AL3, AL4, W6	P12, T10, AF6
VCCIO8	U6, E3, E4	K9, M11, N3
VCC_CKLK1 (2)	AA35	AF18
VCC_CKLK2 (2)	W4	N11
VCC_CKLK3 (2)	T34	AC26
VCC_CKLK4 (2)	R4	P10
VCC_CKOUT1 (7)	U33	AF22
VCC_CKOUT2 (7)	Y1	V7
GND	A1, A18, A35, AK18, AL18, AL30, AL5, AL6, AM18, AM2, AM3, AM31, AM32, AM33, AM34, AM4, AN1, AN18, AN2, AN3, AN34, AN35, AP1, AP18, AP2, AP34, AP35, AR1, AR18, AR35, B1, B18, B2, B34, B35, C18, C2, C3, C33, C34, C35, D17, D18, D2, D3, D32, D33, D34, D4, E18, E30, E31, E32, E33, E5, E6, F18, V1, V2, V3, V30, V31, V32, V33, V34, V4, V5, V6	A2, A8, A14, A19, A25, B1, B2, B6, B21, B25, B26, C3, C13, C24, D4, D23, H8, H19, J9, J18, K10, K17, L11, L13, L16, M12, M15, N1, N4, N13, N14, N26, P1, P2, P3, P13, P14, P23, P26, R12, R15, T11, T16, U10, U17, V9, V18, W8, W19, AC4, AC23, AD3, AD13, AD24, AE1, AE2, AE6, AE21, AE25, AE26, AF2, AF8, AF14, AF19, AF25
GND_CKLK1 (2)	Y30	AE18
GND_CKLK2 (2)	W2	P11
GND_CKLK3 (2)	T33, V35	AC25, N25
GND_CKLK4 (2)	R3	R10
GND_CKOUT1 (7)	U32	AE22
GND_CKOUT2 (7)	Y2	V6
No Connect (N.C.)		A15, A16, B13, B14, B15, B16, C11, C12, C14, C15, C16, AF12, AF15, AE12, AE13, AE14, AE15, AD11, AD12, AD14, AD15, AD16
Total User I/O Pins (11)	488	488

Notes:

(1) This pin can be used as a user I/O pin after configuration.

(2) This pin is the power or ground for the ClockLock and ClockBoost circuitry. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device. VCC_CKLK has the same voltage specifications as the VCCINT and should be connected to a 1.8-V power supply. If the ClockLock or ClockBoost circuitry is not used, this power or ground pin should be connected to VCCINT or GNDINT, respectively.

(3) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.

(4) This pin is the complementary signal for the LVDS pair on dedicated inputs and outputs that can be configured for the LVDS standard. If not used for the LVDS pair, these pins are regular I/O pins. Pins with the "n" suffix carry the negative signal for the LVDS channel. Pins with a "p" suffix carry the positive signal for the LVDS channel.

(5) This pin is a dedicated pin; it is not available as a user I/O pin.

(6) This pin is tri-stated in user mode.

(7) This pin is the power or ground for the external output of a PLL. These pins should be set to the VCCIO level/standard desired for the external clock ouput. To ensure noise resistance, the power and ground supply to the PLL external output should be isolated from the power and ground to the rest of the VCCIO and GNDIO pins. If the PLL or external output is not used, this power or ground pin should be connected to VCCIO or GNDIO, respectively.

(8) The CLKLK_OUT pin is powered by the VCC_CKOUT and GND_CKOUT pins.

(9) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry is locked to the incoming clock and generates an internal clock, LOCK is driven high. LOCK remains high if a periodic clock stops clocking. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.

(10) This pin is the active high enable pin for all of the PLL circuits in the device. When de-asserted, all PLLs are reset to their default, unlocked state and will stop clocking. Once re-asserted, the PLLs will lock again and start clocking. If this pin function is not needed, the pin should be connected to VCCINT.

(11) The user I/O pin count includes dedicated inputs and dedicated clock inputs. It does not include the dedicated clock feedback and output pins.

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
1	1	I/O	–	C6	C5
1	2	I/O	–	B5	D5
–	3	VCCINT	VCCINT	VCCINT	VCCINT
–	4	GNDINT	GND	GND	GND
1	5	I/O	–	A5	E4
1	6	I/O	–	B4	E5
1	7	I/O	–	A4	E6
–	8	VCCIO	VCCIO1	VCCIO1	VCCIO1
–	9	VCCIO	VCCIO8	VCCIO8	VCCIO8
8	10	I/O	–	–	F5
8	11	I/O	F6	E5	F6
8	12	I/O	–	–	G5
8	13	I/O	F5	E3	G6
–	14	VCCINT	VCCINT	VCCINT	VCCINT
–	15	GNDINT	GND	GND	GND
8	16	I/O	–	–	G7
8	17	I/O	–	–	H4
8	18	I/O	F4	F5	H5
8	19	I/O	–	–	H6
8	20	I/O	C1	F4	H7
–	21	GNDIO	GND	GND	GND
8	22	I/O	–	–	J4
8	23	I/O	–	–	J5
8	24	I/O	D1	E4	J6
8	25	I/O	–	–	J7
8	26	I/O	E2	F3	J8
–	27	VCCINT	VCCINT	VCCINT	VCCINT
–	28	GNDINT	GND	GND	GND
8	29	I/O	–	–	K4
8	30	I/O	–	–	K5
8	31	I/O	G6	D5	K6
8	32	I/O	–	–	K7
8	33	I/O	G5	G5	K8
–	34	VCCIO	VCCIO8	VCCIO8	VCCIO8
8	35	I/O	–	–	L5
8	36	I/O	–	–	L6
8	37	I/O	G4	G3	L7
8	38	I/O	–	–	L8
8	39	I/O	G3	G8	M5
–	40	VCCINT	VCCINT	VCCINT	VCCINT
–	41	GNDINT	GND	GND	GND
8	42	I/O	–	–	M6
8	43	I/O	–	–	M7
8	44	I/O	F2	G4	M8
8	45	I/O	–	–	M9
8	46	I/O	E1	C4	M10
–	47	GNDIO	GND	GND	GND
8	48	I/O	–	–	M11

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
8	49	I/O	–	–	N4
8	50	I/O	G2	G6	N5
8	51	I/O	–	–	N6
8	52	I/O	H6	H5	N7
–	53	VCCINT	VCCINT	VCCINT	VCCINT
–	54	GNDINT	GND	GND	GND
8	55	I/O	H4	G7	N8
8	56	I/O	H3	H7	N9
8	57	I/O	F1	H4	N10
8	58	I/O	H2	H6	N11
8	59	I/O	G1	K7	P4
–	60	VCCIO	VCCIO8	VCCIO8	VCCIO8
8	61	I/O	J6	J5	P5
8	62	I/O	J5	H9	P6
8	63	I/O	J4	J8	P7
8	64	I/O	J3	H3	P8
8	65	I/O	J2	K3	P10
–	66	VCCINT	VCCINT	VCCINT	VCCINT
–	67	GNDINT	GND	GND	GND
8	68	I/O	J1	J4	P11
8	69	I/O	K6	K5	R4
8	70	I/O	K5	J6	R5
8	71	I/O	K4	L6	R6
8	72	I/O	K3	J7	R7
–	73	GNDIO	GND	GND	GND
8	74	I/O	K2	J3	R8
8	75	I/O	K1	K8	R10
8	76	I/O, DATA6 (1)	L6	L8	A4
8	77	I/O	L5	K6	R9
8	78	I/O	L4	K4	R11
–	79	VCCINT	VCCINT	VCCINT	VCCINT
–	80	GNDINT	GND	GND	GND
8	81	I/O	L2	N5	T4
8	82	I/O	L1	M8	T5
8	83	I/O, DATA7 (1)	M6	M10	B4
8	84	I/O	M5	M6	T6
8	85	I/O	M4	L7	T7
–	86	VCCIO	VCCIO8	VCCIO8	VCCIO8
8	87	I/O	M3	L9	T8
8	88	I/O	M2	M7	T10
8	89	I/O, nWS (1)	M1	P9	C4
8	90	I/O	N6	L5	T11
8	91	I/O	N5	P8	U4
–	92	VCCINT	VCCINT	VCCINT	VCCINT
–	93	GNDINT	GND	GND	GND
8	94	I/O	N3	L4	U5
8	95	I/O	N2	L3	U6
8	96	I/O, nRS (1)	N1	N10	D4

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
8	97	I/O	P6	R4	U7
8	98	I/O	P5	M5	U8
–	99	GNDIO	GND	GND	GND
8	100	I/O	P4	M3	U9
8	101	I/O	P3	P4	U10
8	102	I/O, nCS (1)	P2	M9	D3
8	103	I/O	P1	R3	U11
8	104	I/O	R6	P5	V4
–	105	VCCINT	VCCINT	VCCINT	VCCINT
–	106	GNDINT	GND	GND	GND
–	107	VCC_CKLK4 (2)	R4	P10	P9
–	108	GND_CKLK4 (2)	R3	R10	T9
–	109	GND_CKLK4 (2)	R3	R10	T9
8	110	I/O, CS (1)	R2	T6	E3
8	111	I/O	R1	M4	V5
8	112	I/O, DEV_CLRn (3)	T6	R9	H3
–	113	VCCIO	VCCIO8	VCCIO8	VCCIO8
8	114	I/O, CLKLK_FB2n (4)	T5	T8	J3
8	115	CLKLK_FB2p	T4	U8	K3
8	116	I/O, CLK4n (4)	T3	R7	N3
8	117	CLK4p	T2	R6	P3
8	118	I/O, CLK2n (4)	T1	N9	R3
–	119	VCCINT	VCCINT	VCCINT	VCCINT
–	120	GNDINT	GND	GND	GND
–	121	DATA0 (5), (6)	U4	N6	V3
–	122	DCLK (5)	U3	N7	W3
8	123	CLK2p	U2	N8	Y3
–	124	nCE (5)	U1	P6	AC3
–	125	TDI (5)	W1	P7	AD3
–	126	GND_CKLK2 (2)	W2	P11	V9
–	127	GND_CKLK2 (2)	W2	P11	V9
–	128	GNDINT	GND	GND	GND
–	129	VCCINT	VCCINT	VCCINT	VCCINT
–	130	VCC_CKLK2 (2)	W4	N11	Y9
7	131	I/O, DEV_OE (3)	Y5	R8	AE3
–	132	VCC_CKOUT2 (7)	Y1	V7	AA9
–	133	GND_CKOUT2 (7)	Y2	V6	W9
–	134	CLKLK_OUT2p (8)	Y3	T7	AH3
7	135	I/O, CLKLK_OUT2n (4)	Y4	U7	AJ3
–	136	GNDIO	GND	GND	GND
7	137	I/O, LVDSTXINCLK1p	W5	D1	AM5
7	138	I/O, LVDSTXINCLK1n (4)	Y6	D2	AL5
7	139	I/O, LOCK2 (9)	AB6	U6	AK4

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
7	140	I/O, LVDSTXOUTCLK1n (4)	AA2	E1	AM4
7	141	I/O, LVDSTXOUTCLK1p	AA3	E2	AL4
–	142	GNDINT	GND	GND	GND
–	143	VCCINT	VCCINT	VCCINT	VCCINT
7	144	I/O, LVDSTX01p	AA5	F1	D1
7	145	I/O, LVDSTX01n (4)	AA6	F2	D2
7	146	I/O	AA1	R5	V6
7	147	I/O, LVDSTX02n (4)	AB2	G1	E1
7	148	I/O, LVDSTX02p	AB3	G2	E2
–	149	VCCIO	VCCIO7	VCCIO7	VCCIO7
7	150	I/O, LVDSTX03p	AB4	H1	H1
7	151	I/O, LVDSTX03n (4)	AB5	H2	H2
7	152	I/O	AB1	T5	V7
7	153	I/O, LVDSTX04n (4)	AC1	J1	J1
7	154	I/O, LVDSTX04p	AC2	J2	J2
–	155	GNDINT	GND	GND	GND
–	156	VCCINT	VCCINT	VCCINT	VCCINT
7	157	I/O, LVDSTX05p	AC4	K1	K1
7	158	I/O, LVDSTX05n (4)	AC5	K2	K2
7	159	I/O, LOCK4 (9)	AC6	W7	AK5
7	160	I/O, LVDSTX06n (4)	AD1	L1	N1
7	161	I/O, LVDSTX06p	AD2	L2	N2
–	162	GNDIO	GND	GND	GND
7	163	I/O, LVDSTX07p	AD3	M1	P1
7	164	I/O, LVDSTX07n (4)	AD4	M2	P2
7	165	I/O	AD5	T3	V8
7	166	I/O, LVDSTX08n (4)	AD6	R1	R1
7	167	I/O, LVDSTX08p	AE1	R2	R2
–	168	GNDINT	GND	GND	GND
–	169	VCCINT	VCCINT	VCCINT	VCCINT
7	170	I/O, LVDSTX09p	AE3	T1	V1
7	171	I/O, LVDSTX09n (4)	AE4	T2	V2
7	172	I/O	AE5	U5	V10
7	173	I/O, LVDSTX10n (4)	AE6	U1	W1
7	174	I/O, LVDSTX10p	AF1	U2	W2
–	175	VCCIO	VCCIO7	VCCIO7	VCCIO7
7	176	I/O, LVDSTX11p	AF2	V1	Y1
7	177	I/O, LVDSTX11n (4)	AF3	V2	Y2
7	178	I/O	AF4	T4	V11
7	179	I/O, LVDSTX12n (4)	AF5	W1	AC1
7	180	I/O, LVDSTX12p	AF6	W2	AC2
–	181	GNDINT	GND	GND	GND
–	182	VCCINT	VCCINT	VCCINT	VCCINT
7	183	I/O, LVDSTX13p	AH1	Y1	AD1
7	184	I/O, LVDSTX13n (4)	AG2	Y2	AD2
7	185	I/O	AG3	U4	W4

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
7	186	I/O, LVDSTX14n (4)	AG4	AA1	AE1
7	187	I/O, LVDSTX14p	AG5	AA2	AE2
–	188	GNDIO	GND	GND	GND
7	189	I/O, LVDSTX15p	AG6	AB1	AH1
7	190	I/O, LVDSTX15n (4)	AJ1	AB2	AH2
7	191	I/O	AH2	W4	W5
7	192	I/O, LVDSTX16n (4)	AK1	AC1	AJ1
7	193	I/O, LVDSTX16p	AH3	AC2	AJ2
–	194	GNDINT	GND	GND	GND
–	195	VCCINT	VCCINT	VCCINT	VCCINT
7	196	I/O	AH5	U3	W6
7	197	I/O	–	–	W7
7	198	I/O	AH6	V3	W8
7	199	I/O	–	–	W10
7	200	I/O	–	–	W11
–	201	VCCIO	VCCIO7	VCCIO7	VCCIO7
7	202	I/O	AJ2	W5	Y4
7	203	I/O	–	–	Y5
7	204	I/O	AL1	W6	Y6
7	205	I/O	–	–	Y7
7	206	I/O	–	–	Y8
–	207	GNDINT	GND	GND	GND
–	208	VCCINT	VCCINT	VCCINT	VCCINT
7	209	I/O	AK2	V5	Y10
7	210	I/O	–	–	Y11
7	211	I/O	AJ3	V4	AA5
7	212	I/O	–	–	AA6
7	213	I/O	–	–	AA7
–	214	GNDIO	GND	GND	GND
7	215	I/O	AJ4	W3	AA8
7	216	I/O	–	–	AA10
7	217	I/O	AJ5	Y5	AA11
7	218	I/O	–	–	AB5
7	219	I/O	–	–	AB6
–	220	GNDINT	GND	GND	GND
–	221	VCCINT	VCCINT	VCCINT	VCCINT
7	222	I/O	AJ6	AB5	AB7
7	223	I/O	–	–	AC4
7	224	I/O	AM1	AA5	AC5
7	225	I/O	–	–	AC6
7	226	I/O	–	–	AC7
–	227	VCCIO	VCCIO7	VCCIO7	VCCIO7
7	228	I/O	AK3	Y6	AD4
7	229	I/O	–	–	AD5
7	230	I/O	AK4	AA6	AD6
7	231	I/O	–	–	AD7
7	232	I/O	–	–	AE4
–	233	GNDINT	GND	GND	GND

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
–	234	VCCINT	VCCINT	VCCINT	VCCINT
7	235	I/O	AK5	AA7	AE5
7	236	I/O	–	–	AE6
7	237	I/O	AK6	AB6	AE7
7	238	I/O	–	–	AF5
–	239	GNDIO	GND	GND	GND
6	240	I/O	–	AB4	AF6
6	241	I/O	–	AA4	AG5
6	242	I/O	–	AC5	AG6
–	243	GNDINT	GND	GND	GND
–	244	VCCINT	VCCINT	VCCINT	VCCINT
6	245	I/O	–	Y4	AH4
6	246	I/O	–	AE4	AH5
–	247	VCCIO	VCCIO6	VCCIO6	VCCIO6
6	248	I/O	AL7	AB3	AJ4
6	249	I/O	AM6	AF4	AJ5
6	250	I/O	AP3	Y3	AH6
6	251	I/O	AN5	AD4	AF7
6	252	I/O	AR2	AA3	AG7
6	253	I/O	AP4	AE5	AH7
6	254	I/O	AL8	AD5	AE8
6	255	I/O	AM7	AD6	AF8
6	256	I/O	AN6	AB7	AG8
6	257	I/O	AR3	Y7	AH8
–	258	GNDIO	GND	GND	GND
6	259	I/O	AP5	AC6	AJ8
6	260	I/O	AL9	AB8	AK8
6	261	I/O	AR4	AF5	AL8
6	262	I/O	AM8	V8	AM8
6	263	I/O	AN7	AC7	AE9
6	264	I/O	AP6	AD7	AF9
6	265	I/O	AR5	T9	AG9
6	266	I/O	AM9	AE7	AH9
6	267	I/O	AL10	AA9	AJ9
6	268	I/O	AN8	AF7	AK9
–	269	VCCIO	VCCIO6	VCCIO6	VCCIO6
6	270	I/O	AP7	AA8	AL9
6	271	I/O	AR6	AC8	AM9
6	272	I/O	AM10	Y8	AE10
6	273	I/O	AN9	AD8	AF10
6	274	I/O	AL11	Y9	AG10
6	275	I/O	AP8	W9	AH10
6	276	I/O	AR7	AB9	AJ10
6	277	I/O	AM11	W10	AK10
6	278	I/O	AN10	AC9	AL10
6	279	I/O	AP9	Y10	AE11
–	280	GNDIO	GND	GND	GND
–	281	VCCINT	VCCINT	VCCINT	VCCINT

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
–	282	VCCINT	VCCINT	VCCINT	VCCINT
–	283	GNDINT	GND	GND	GND
–	284	GNDINT	GND	GND	GND
6	285	I/O	AR8	AD9	AF11
6	286	I/O	AN11	AA10	AG11
6	287	I/O	AP10	AB11	AH11
6	288	I/O	AR9	V11	AE12
6	289	I/O	AL13	AB10	AF12
6	290	I/O	AM13	AC10	AG12
6	291	I/O	AN12	AA11	AH12
6	292	I/O	AP11	AE9	AE13
6	293	I/O	AL14	Y11	AF13
6	294	I/O	AR10	AF9	AG13
–	295	VCCIO	VCCIO6	VCCIO6	VCCIO6
6	296	I/O	AN13	W11	AH13
6	297	I/O	AP12	AF11	AJ13
6	298	I/O	AM14	V12	AK13
6	299	I/O	AR11	AE10	AL13
6	300	I/O	AL15	W12	AF14
6	301	I/O	AN14	Y12	AG14
6	302	I/O	AP13	T13	AH14
6	303	I/O	AR12	W14	AJ14
6	304	I/O	AR13	AB12	AK14
6	305	I/O	AM15	AF10	AL14
–	306	GNDIO	GND	GND	GND
6	307	I/O	AN15	U13	AF15
6	308	I/O	AL16	W13	AG15
6	309	I/O	AP14	AE11	AH15
6	310	I/O	AR14	V13	AJ15
6	311	I/O	AP15	AD11	AK15
6	312	I/O	AR15	AD12	AL15
6	313	I/O, LVDSDESKEW	AM16	U12	AM10
6	314	I/O	AN16	AE12	AF16
6	315	I/O	AP16	AF12	AG16
6	316	I/O	AR16	AE13	AH16
–	317	VCCIO	VCCIO6	VCCIO6	VCCIO6
–	318	CONF_DONE (5)	AM17	AA12	AM13
–	319	nSTATUS (5)	AN17	AA13	AM14
5	320	FAST4	AP17	Y13	AM15
–	321	VCCIO	VCCIO5	VCCIO5	VCCIO5
–	322	VCCINT	VCCINT	VCCINT	VCCINT
–	323	VCCINT	VCCINT	VCCINT	VCCINT
–	324	GNDINT	GND	GND	GND
–	325	GNDINT	GND	GND	GND
5	326	FAST3	AP19	Y14	AM18
–	327	TCK (5)	AN19	AA14	AM19
–	328	TMS (5)	AM19	AA15	AM20
5	329	I/O	AR20	AE14	AJ16

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
5	330	I/O	AP20	AD14	AK16
5	331	I/O	AN20	AE15	AK17
5	332	I/O	AM20	AD15	AJ17
5	333	I/O	AR21	AD16	AH17
5	334	I/O	AP21	AC13	AG17
5	335	I/O	AR22	AD17	AF17
5	336	I/O	AP22	AC12	AL18
5	337	I/O	AL20	AC14	AK18
5	338	I/O	AN21	AD10	AJ18
–	339	GNDIO	GND	GND	GND
5	340	I/O	AM21	AB13	AH18
5	341	I/O	AR23	V14	AG18
5	342	I/O	AR24	AB14	AF18
5	343	I/O	AP23	Y15	AL19
5	344	I/O	AN22	AC11	AK19
5	345	I/O	AL21	AD18	AJ19
5	346	I/O	AR25	U14	AH19
5	347	I/O	AM22	AC15	AG19
5	348	I/O	AP24	V15	AF19
5	349	I/O	AN23	AB15	AL20
–	350	VCCIO	VCCIO5	VCCIO5	VCCIO5
5	351	I/O	AR26	W15	AK20
5	352	I/O	AL22	AB16	AJ20
5	353	I/O	AP25	T14	AH20
5	354	I/O	AN24	AD19	AG20
5	355	I/O	AM23	AA16	AF20
5	356	I/O	AL23	Y16	AE20
5	357	I/O	AR27	AC16	AH21
5	358	I/O	AP26	W16	AG21
5	359	I/O	AN25	AC17	AF21
5	360	I/O	AR28	U15	AE21
–	361	VCCINT	VCCINT	VCCINT	VCCINT
–	362	VCCINT	VCCINT	VCCINT	VCCINT
–	363	GNDINT	GND	GND	GND
–	364	GNDINT	GND	GND	GND
–	365	GNDIO	GND	GND	GND
5	366	I/O	AP27	AB17	AH22
5	367	I/O	AN26	V16	AG22
5	368	I/O	AM25	AE16	AF22
5	369	I/O	AR29	AA17	AE22
5	370	I/O	AP28	AD20	AM23
5	371	I/O	AL25	AB18	AL23
5	372	I/O	AN27	Y17	AK23
5	373	I/O	AM26	AF16	AJ23
5	374	I/O	AR30	AA18	AH23
5	375	I/O	AP29	AC18	AG23
–	376	VCCIO	VCCIO5	VCCIO5	VCCIO5
5	377	I/O	AN28	W17	AF23

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
5	378	I/O	AL26	AE17	AE23
5	379	I/O	AM27	Y18	AM24
5	380	I/O	AR31	AF17	AL24
5	381	I/O	AP30	W18	AK24
5	382	I/O	AN29	AA19	AJ24
5	383	I/O	AM28	AD21	AH24
5	384	I/O	AR32	Y19	AG24
5	385	I/O	AL27	AD22	AF24
5	386	I/O	AP31	W20	AE24
–	387	GNDIO	GND	GND	GND
5	388	I/O	AR33	AC19	AM25
5	389	I/O	AN30	Y20	AL25
5	390	I/O	AM29	AB20	AK25
5	391	I/O	AL28	AB19	AJ25
5	392	I/O	AP32	AC20	AH25
5	393	I/O	AR34	AD23	AG25
5	394	I/O	AN31	AA20	AF25
5	395	I/O	AP33	AB24	AE25
5	396	I/O	AM30	AC22	AH26
5	397	I/O	AL29	AC21	AG26
–	398	VCCIO	VCCIO5	VCCIO5	VCCIO5
5	399	I/O	–	Y23	AF26
5	400	I/O	–	Y24	AH27
–	401	VCCINT	VCCINT	VCCINT	VCCINT
–	402	GNDINT	GND	GND	GND
5	403	I/O	–	AA23	AK28
5	404	I/O	–	AA24	AK29
5	405	I/O	–	AB23	AJ28
–	406	GNDIO	GND	GND	GND
4	407	I/O	–	–	AJ29
4	408	I/O	AL33	AA21	AJ30
4	409	I/O	–	–	AH28
4	410	I/O	AK30	Y22	AH29
–	411	VCCINT	VCCINT	VCCINT	VCCINT
–	412	GNDINT	GND	GND	GND
4	413	I/O	–	–	AH30
4	414	I/O	–	–	AG27
4	415	I/O	AK31	AB21	AG28
4	416	I/O	–	–	AF27
4	417	I/O	AK32	U19	AF28
–	418	VCCIO	VCCIO4	VCCIO4	VCCIO4
4	419	I/O	–	–	AE26
4	420	I/O	–	–	AE27
4	421	I/O	AL34	AB22	AE28
4	422	I/O	–	–	AE29
4	423	I/O	AM35	V19	AE30
–	424	VCCINT	VCCINT	VCCINT	VCCINT
–	425	GNDINT	GND	GND	GND

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
4	426	I/O	–	–	AD26
4	427	I/O	–	–	AD27
4	428	I/O	AJ30	T18	AD28
4	429	I/O	–	–	AD29
4	430	I/O	AJ31	W21	AD30
–	431	GNDIO	GND	GND	GND
4	432	I/O	–	–	AC26
4	433	I/O	–	–	AC27
4	434	I/O	AJ32	V20	AC28
4	435	I/O	–	–	AC29
4	436	I/O	AJ33	V21	AB26
–	437	VCCINT	VCCINT	VCCINT	VCCINT
–	438	GNDINT	GND	GND	GND
4	439	I/O	–	–	AB27
4	440	I/O	–	–	AB28
4	441	I/O	AK34	Y21	AA22
4	442	I/O	–	–	AA23
4	443	I/O	AL35	W22	AA24
–	444	VCCIO	VCCIO4	VCCIO4	VCCIO4
4	445	I/O	–	–	AA25
4	446	I/O	–	–	AA26
4	447	I/O	AJ34	AA22	AA27
4	448	I/O	–	–	AA28
4	449	I/O	AH30	U20	Y22
–	450	VCCINT	VCCINT	VCCINT	VCCINT
–	451	GNDINT	GND	GND	GND
4	452	I/O	AH32	R17	Y23
4	453	I/O	AH33	W23	Y24
4	454	I/O	AK35	T19	Y25
4	455	I/O	AH34	U21	Y26
4	456	I/O	AJ35	P17	Y27
–	457	GNDIO	GND	GND	GND
4	458	I/O	AG30	R18	Y28
4	459	I/O	AG31	W24	Y29
4	460	I/O	AG32	T20	W22
4	461	I/O	AG33	V24	W23
4	462	I/O	AG34	N16	W25
–	463	VCCINT	VCCINT	VCCINT	VCCINT
–	464	GNDINT	GND	GND	GND
4	465	I/O	AG35	V22	W26
4	466	I/O	AF30	R19	W27
4	467	I/O	AF31	V23	W28
4	468	I/O	AF32	P18	W29
4	469	I/O	AF33	N17	V22
–	470	VCCIO	VCCIO4	VCCIO4	VCCIO4
4	471	I/O	AF34	T21	V23
4	472	I/O	AF35	R21	V25
4	473	I/O	AE30	U22	V26

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
4	474	I/O	AE31	R20	V27
4	475	I/O	AE32	P22	V28
–	476	VCCINT	VCCINT	VCCINT	VCCINT
–	477	GNDINT	GND	GND	GND
4	478	I/O	AE34	N18	V29
4	479	I/O	AE35	U23	U22
4	480	I/O	AD30	N19	U23
4	481	I/O	AD31	N22	U24
4	482	I/O	AD32	L20	U25
–	483	GNDIO	GND	GND	GND
4	484	I/O	AD33	M17	U26
4	485	I/O	AD34	T22	U27
4	486	I/O	AD35	M18	U28
4	487	I/O	AC30	T23	U29
4	488	I/O	AC31	R23	T22
–	489	VCCINT	VCCINT	VCCINT	VCCINT
–	490	GNDINT	GND	GND	GND
4	491	I/O	AC33	U24	T23
4	492	I/O	AC34	R24	T25
4	493	I/O	AC35	T24	T26
4	494	I/O	AB30	M21	T27
4	495	I/O	AB31	M24	T28
–	496	VCCIO	VCCIO4	VCCIO4	VCCIO4
4	497	I/O	AB32	M22	T29
4	498	I/O	AB33	R22	R22
4	499	I/O	AB34	M23	R23
4	500	I/O	AB35	L22	R24
4	501	I/O, LOCK1 (9)	AA30	L21	AC30
–	502	VCCINT	VCCINT	VCCINT	VCCINT
–	503	GNDINT	GND	GND	GND
4	504	I/O	AA32	L23	R25
4	505	I/O	AA33	L24	R26
4	506	I/O	AA34	N23	R27
–	507	VCC_CKLK1 (2)	AA35	AF18	W24
–	508	GND_CKLK1 (2)	Y30	AE18	V24
–	509	GND_CKLK1 (2)	Y30	AE18	V24
–	510	GNDIO	GND	GND	GND
4	511	I/O, CLKLK_FB1n (4)	Y31	AF20	AM28
4	512	CLKLK_FB1p	Y32	AE20	AL28
4	513	I/O, CLK3n (4)	Y33	M20	Y30
4	514	CLK3p	Y34	M19	W30
4	515	I/O, CLK1n (4)	Y35	P19	V30
–	516	VCCINT	VCCINT	VCCINT	VCCINT
–	517	GNDINT	GND	GND	GND
–	518	nCONFIG (5)	W32	P21	R30
–	519	CLKLK_ENA (5), (10)	W33	P16	P30

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
4	520	CLK1p	W34	P20	N30
–	521	MSEL1 (5)	W35	N20	K30
–	522	MSEL0 (5)	U35	N21	J30
–	523	GNDINT	GND	GND	GND
–	524	VCCINT	VCCINT	VCCINT	VCCINT
–	525	VCC_CKOUT1 (7)	U33	AF22	N24
–	526	GND_CKOUT1 (7)	U32	AE22	T24
–	527	CLKLK_OUT1p (8)	U31	AE23	AM29
3	528	I/O, CLKLK_OUT1n (4)	T35	AF23	AL29
–	529	VCC_CKLK3 (2)	T34	AC26	M24
–	530	VCCIO	VCCIO3	VCCIO3	VCCIO3
–	531	GND_CKLK3 (2)	V35	N25	P23
–	532	GND_CKLK3 (2)	T33	AC25	P24
3	533	I/O, LVDSRXINCLK1p	T32	AB25	B29
3	534	I/O, LVDSRXINCLK1n	T31	AB26	A29
3	535	I/O	T30	J23	R28
3	536	I/O	R35	L19	R29
–	537	GNDINT	GND	GND	GND
–	538	VCCINT	VCCINT	VCCINT	VCCINT
3	539	I/O, LVDSRX01p	R33	AA25	AJ32
3	540	I/O, LVDSRX01n (4)	R32	AA26	AJ31
3	541	I/O, LOCK3 (9)	R31	L18	H30
3	542	I/O, LVDSRX02n (4)	R30	Y25	AH32
3	543	I/O, LVDSRX02p	P35	Y26	AH31
–	544	GNDIO	GND	GND	GND
3	545	I/O, LVDSRX03p	P34	W25	AE32
3	546	I/O, LVDSRX03n (4)	P33	W26	AE31
3	547	I/O	P32	J24	P22
3	548	I/O, LVDSRX04n (4)	P31	V25	AD32
3	549	I/O, LVDSRX04p	P30	V26	AD31
–	550	GNDINT	GND	GND	GND
–	551	VCCINT	VCCINT	VCCINT	VCCINT
3	552	I/O, LVDSRX05p	N34	U25	AC32
3	553	I/O, LVDSRX05n (4)	N33	U26	AC31
3	554	I/O	N32	K21	P25
3	555	I/O, LVDSRX06n (4)	N31	T25	Y32
3	556	I/O, LVDSRX06p	N30	T26	Y31
–	557	VCCIO	VCCIO3	VCCIO3	VCCIO3
3	558	I/O, LVDSRX07p	M35	R25	W32
3	559	I/O, LVDSRX07n (4)	M34	R26	W31
3	560	I/O	M33	K23	P26
3	561	I/O, LVDSRX08n (4)	M32	M25	V32
3	562	I/O, LVDSRX08p	M31	M26	V31
–	563	GNDINT	GND	GND	GND
–	564	VCCINT	VCCINT	VCCINT	VCCINT
3	565	I/O, LVDSRX09p	L35	L25	R32

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
3	566	I/O, LVDSRX09n (4)	L34	L26	R31
3	567	I/O	L33	K20	P27
3	568	I/O, LVDSRX10n (4)	L32	K25	P32
3	569	I/O, LVDSRX10p	L31	K26	P31
–	570	GNDIO	GND	GND	GND
3	571	I/O, LVDSRX11p	L30	J25	N32
3	572	I/O, LVDSRX11n (4)	K35	J26	N31
3	573	I/O	K34	K22	P28
3	574	I/O, LVDSRX12n (4)	K33	H25	K32
3	575	I/O, LVDSRX12p	K32	H26	K31
–	576	GNDINT	GND	GND	GND
–	577	VCCINT	VCCINT	VCCINT	VCCINT
3	578	I/O, LVDSRX13p	K30	G25	J32
3	579	I/O, LVDSRX13n (4)	J35	G26	J31
3	580	I/O	H35	K24	P29
3	581	I/O, LVDSRX14n (4)	J34	F25	H32
3	582	I/O, LVDSRX14p	J33	F26	H31
–	583	VCCIO	VCCIO3	VCCIO3	VCCIO3
3	584	I/O, LVDSRX15p	J32	E25	E32
3	585	I/O, LVDSRX15n (4)	J31	E26	E31
3	586	I/O	J30	H24	N22
3	587	I/O, LVDSRX16n (4)	G35	D25	D32
3	588	I/O, LVDSRX16p	H34	D26	D31
–	589	GNDINT	GND	GND	GND
–	590	VCCINT	VCCINT	VCCINT	VCCINT
3	591	I/O	H33	K19	N23
3	592	I/O	–	–	N25
3	593	I/O	H32	J20	N26
3	594	I/O	–	–	N27
3	595	I/O	–	–	N28
–	596	GNDIO	GND	GND	GND
3	597	I/O	H31	G22	N29
3	598	I/O	–	–	M22
3	599	I/O	H30	H20	M23
3	600	I/O	–	–	M25
3	601	I/O	–	–	M26
–	602	GNDINT	GND	GND	GND
–	603	VCCINT	VCCINT	VCCINT	VCCINT
3	604	I/O	G34	H22	M27
3	605	I/O	–	–	M28
3	606	I/O	E35	J22	L26
3	607	I/O	–	–	L27
3	608	I/O	–	–	L28
–	609	VCCIO	VCCIO3	VCCIO3	VCCIO3
3	610	I/O	F34	G24	K26
3	611	I/O	–	–	K27
3	612	I/O	G33	H21	K28
3	613	I/O	–	–	K29

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
3	614	I/O	–	–	J26
–	615	GNDINT	GND	GND	GND
–	616	VCCINT	VCCINT	VCCINT	VCCINT
3	617	I/O	G32	G21	J27
3	618	I/O	–	–	J28
3	619	I/O	G31	J21	J29
3	620	I/O	–	–	H26
3	621	I/O	–	–	H27
–	622	GNDIO	GND	GND	GND
3	623	I/O	D35	F22	H28
3	624	I/O	–	–	H29
3	625	I/O	E34	G20	G27
3	626	I/O	–	–	G28
3	627	I/O	–	–	F28
–	628	GNDINT	GND	GND	GND
–	629	VCCINT	VCCINT	VCCINT	VCCINT
3	630	I/O	F33	F21	E28
3	631	I/O	–	–	E29
3	632	I/O	F32	E22	E30
3	633	I/O	–	–	D28
–	634	VCCIO	VCCIO3	VCCIO3	VCCIO3
–	635	VCCIO	VCCIO2	VCCIO2	VCCIO2
2	636	I/O	–	E23	D29
2	637	I/O	–	D22	D30
2	638	I/O	–	F24	C28
–	639	GNDINT	GND	GND	GND
–	640	VCCINT	VCCINT	VCCINT	VCCINT
2	641	I/O	–	E24	C29
2	642	I/O	–	H23	B28
–	643	GNDIO	GND	GND	GND
2	644	I/O	E29	C23	A28
2	645	I/O	D30	G23	F27
2	646	I/O	B33	C22	E27
2	647	I/O	C31	F23	G26
2	648	I/O	A34	B23	F26
2	649	I/O	B32	A23	E26
2	650	I/O	E28	E21	H25
2	651	I/O	D29	B22	G25
2	652	I/O	C30	F20	F25
2	653	I/O	A33	D21	E25
–	654	VCCIO	VCCIO2	VCCIO2	VCCIO2
2	655	I/O	B31	C21	D25
2	656	I/O	E27	E20	C25
2	657	I/O	A32	J19	B25
2	658	I/O	D28	A22	A25
2	659	I/O	C29	G19	H24
2	660	I/O	B30	F19	G24
2	661	I/O	A31	E19	F24

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
2	662	I/O	D27	K18	E24
2	663	I/O	E26	D20	D24
2	664	I/O	C28	H18	C24
–	665	GNDIO	GND	GND	GND
2	666	I/O	B29	C20	B24
2	667	I/O	A30	G18	H23
2	668	I/O	D26	D19	G23
2	669	I/O	C27	E18	F23
2	670	I/O	E25	B20	E23
2	671	I/O	B28	A20	D23
2	672	I/O	A29	F18	C23
2	673	I/O	D25	C19	B23
2	674	I/O	C26	E17	H22
2	675	I/O	B27	D18	G22
–	676	VCCIO	VCCIO2	VCCIO2	VCCIO2
–	677	GNDINT	GND	GND	GND
–	678	GNDINT	GND	GND	GND
–	679	VCCINT	VCCINT	VCCINT	VCCINT
–	680	VCCINT	VCCINT	VCCINT	VCCINT
–	681	GNDINT	–	–	–
2	682	I/O	A28	F17	F22
2	683	I/O	C25	C18	E22
2	684	I/O	B26	G17	H21
2	685	I/O	A27	B18	G21
2	686	I/O	E23	H17	F21
2	687	I/O	D23	F16	E21
2	688	I/O	C24	D17	H20
2	689	I/O	B25	J17	G20
2	690	I/O	E22	E16	F20
2	691	I/O	A26	G16	E20
–	692	GNDIO	GND	GND	GND
2	693	I/O	C23	A18	D20
2	694	I/O	B24	H16	C20
2	695	I/O	D22	C17	B20
2	696	I/O	A25	E15	G19
2	697	I/O	E21	D16	F19
2	698	I/O	C22	B17	E19
2	699	I/O	B23	F15	D19
2	700	I/O	A24	A17	C19
2	701	I/O	A23	E14	B19
2	702	I/O	D21	H15	G18
–	703	VCCIO	VCCIO2	VCCIO2	VCCIO2
2	704	I/O	C21	E13	F18
2	705	I/O	E20	L14	E18
2	706	I/O	B22	G15	D18
2	707	I/O	A22	K15	C18
2	708	I/O	B21	J16	B18
2	709	I/O	A21	C16	G17

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
2	710	I/O	D20	B16	F17
2	711	I/O	C20	C15	E17
2	712	I/O	B20	B15	D17
2	713	I/O	A20	A15	C17
–	714	TRST (5)	D19	F14	A24
–	715	NCEO (5)	C19	G14	A23
1	716	FAST1	B19	H14	A20
–	717	GNDINT	GND	GND	GND
–	718	GNDINT	GND	GND	GND
–	719	VCCINT	VCCINT	VCCINT	VCCINT
–	720	VCCINT	VCCINT	VCCINT	VCCINT
–	721	GNDIO	GND	GND	GND
1	722	FAST2	B17	F13	A19
–	723	TDO (5)	C17	G13	A18
–	724	GNDINT	GND	GND	–
1	725	I/O	A16	C14	C16
1	726	I/O	B16	B14	D16
1	727	I/O, INITDONE (3)	C16	J15	A15
1	728	I/O	D16	C12	E16
1	729	I/O	A15	B13	F16
1	730	I/O	B15	C11	G16
1	731	I/O, RDYnBSY (1)	A14	J14	A14
1	732	I/O	B14	D15	B15
1	733	I/O	E16	D14	C15
1	734	I/O, CLKUSR (1)	C15	K14	A13
–	735	VCCIO	VCCIO1	VCCIO1	VCCIO1
1	736	I/O	D15	A12	D15
1	737	I/O	A13	D13	E15
1	738	I/O	A12	B11	F15
1	739	I/O	B13	B12	G15
1	740	I/O	C14	H13	B14
1	741	I/O	E15	F12	C14
1	742	I/O	A11	A11	D14
1	743	I/O	D14	E12	E14
1	744	I/O	B12	A10	F14
1	745	I/O, DATA1 (1)	C13	K13	A10
–	746	GNDIO	GND	GND	GND
1	747	I/O	A10	D12	G14
1	748	I/O	E14	D11	B13
1	749	I/O	B11	E11	C13
1	750	I/O	C12	B10	D13
1	751	I/O	D13	C10	E13
1	752	I/O	E13	J13	F13
1	753	I/O	A9	D10	G13
1	754	I/O	B10	H12	E12
1	755	I/O	C11	E10	F12
1	756	I/O, DATA2 (1)	A8	J12	A9
–	757	GNDINT	GND	GND	GND

I/O & VREF Bank	Pad Number Orientation	Pin/Pad Function	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
–	758	GNDINT	GND	GND	GND
–	759	VCCINT	VCCINT	VCCINT	VCCINT
–	760	VCCINT	VCCINT	VCCINT	VCCINT
–	761	VCCIO	VCCIO1	VCCIO1	VCCIO1
1	762	I/O	B9	F11	G12
1	763	I/O	C10	B9	E11
1	764	I/O	D11	G12	F11
1	765	I/O	A7	C9	G11
1	766	I/O	B8	G11	B10
1	767	I/O	E11	E9	C10
1	768	I/O	C9	F9	D10
1	769	I/O	D10	D9	E10
1	770	I/O	A6	K12	F10
1	771	I/O, DATA3 (1)	B7	F10	A8
–	772	GNDIO	GND	GND	GND
1	773	I/O	C8	A9	G10
1	774	I/O	E10	H11	H10
1	775	I/O	D9	D8	B9
1	776	I/O	A5	E8	C9
1	777	I/O	B6	C8	D9
1	778	I/O	C7	F8	E9
1	779	I/O	D8	E7	F9
1	780	I/O	A4	G10	G9
1	781	I/O	E9	C7	H9
1	782	I/O, DATA4 (1)	B5	G9	B5
–	783	VCCIO	VCCIO1	VCCIO1	VCCIO1
1	784	I/O	A3	H10	B8
1	785	I/O	C6	B7	C8
1	786	I/O	D7	J11	D8
1	787	I/O	E8	D7	E8
1	788	I/O	B4	D6	F8
1	789	I/O	A2	A7	G8
1	790	I/O	C5	F7	H8
1	791	I/O	B3	E6	E7
1	792	I/O	D6	C5	F7
1	793	I/O, DATA5 (1)	E7	F6	A5
–	794	GNDIO	GND	GND	GND
–	795	–	–	–	–

Pin Name	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
MSEL0 (5)	U35	N21	J30
MSEL1 (5)	W35	N20	K30
nSTATUS (5)	AN17	AA13	AM14
nCONFIG (5)	W32	P21	R30
DCLK (5)	U3	N7	W3
CONF_DONE (5)	AM17	AA12	AM13
INIT_DONE (3)	C16	J15	A15
nCE (5)	U1	P6	AC3
nCEO (5)	C19	G14	A23
nWS (1)	M1	P9	C4
nRS (1)	N1	N10	D4
nCS (1)	P2	M9	D3
CS (1)	R2	T6	E3
RDYnBSY (1)	A14	J14	A14
CLKUSR (1)	C15	K14	A13
DATA7 (1)	M6	M10	B4
DATA6 (1)	L6	L8	A4
DATA5 (1)	E7	F6	A5
DATA4 (1)	B5	G9	B5
DATA3 (1)	B7	F10	A8
DATA2 (1)	A8	J12	A9
DATA1 (1)	C13	K13	A10
DATA0 (5), (6)	U4	N6	V3
TDI (5)	W1	P7	AD3
TDO (5)	C17	G13	A18
TCK (5)	AN19	AA14	AM19
TMS (5)	AM19	AA15	AM20
TRST (5)	D19	F14	A24
Dedicated Fast I/Os	AP19, AP17, B17, B19	Y14, Y13, F13, H14	AM18, AM15, A19, A20
CLK1p	W34	P20	N30
CLK2p	U2	N8	Y3
CLK3p	Y34	M19	W30
CLK4p	T2	R6	P3
LOCK1 (9)	AA30	L21	AC30
LOCK2 (9)	AB6	U6	AK4
LOCK3 (9)	R31	L18	H30
LOCK4 (9)	AC6	W7	AK5
CLKLK_ENA (5), (10)	W33	P16	P30
CLKLK_OUT1p (8)	U31	AE23	AM29
CLKLK_OUT2p (8)	Y3	T7	AH3
CLKLK_FB1p	Y32	AE20	AL28
CLKLK_FB2p	T4	U8	K3
DEV_CLRn (3)	T6	R9	H3
DEV_OE (3)	Y5	R8	AE3

Pin Name	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
VCCINT	A17, A19, AA31, AA4, AC3, AC32, AE2, AE33, AG1, AH31, AH35, AH4, AK33, AL12, AL2, AL24, AM12, AM24, AR17, AR19, D12, D24, E12, E24, F3, F35, G30, H1, H5, K31, L3, M30, N35, N4, R34, R5, U34, U5, W3, W31	A3, A24, B3, B8, B19, B24, C1, C2, C25, C26, D3, D24, K11, L10, L15, M13, M16, N2, N12, P15, P24, P25, R11, R14, T12, T17, U9, U16, AC3, AC24, AD1, AD2, AD25, AD26, AE3, AE8, AE19, AE24, AF3, AF24	A2, B1, F1, F2, L1, L2, U1, U2, U3, AB1, AB2, AG1, AG2, AL1, AM2, AL6, AM6, AL11, AM11, AL17, AM17, AL22, AM22, AL27, AM27, AM31, AL32, AG31, AG32, AB31, AB32, T30, T31, T32, L31, L32, F31, F32, B32, A31, A27, B27, A22, B22, A16, B16, A11, B11, A6, B6
VCCIO1	C4, D5, E17	A6, J10, L12	A12, B12, A7, B7, A3
VCCIO2	E19, D31, C32	A13, K16,M14, A16	A30, A26, B26, A21, B21
VCCIO3	F30, F31, U30	A21, L17, N15	M31, M32, G31, G32, C32
VCCIO4	W30, AL31, AL32	N24, R16, U18	AK32, AF31, AF32, AA31, AA32
VCCIO5	AN32, AN33, AL19	T15, V17, AF21	AL21, AM21, AL26, AM26, AM30
VCCIO6	AL17, AM5, AN4	R13, U11, V10, AF13	AM3, AL7, AM7, AL12, AM12
VCCIO7	AL3, AL4, W6	P12, T10, AF6	AA1, AA2, AF1, AF2, AK1
VCCIO8	U6, E3, E4	K9, M11, N3	C1, G1, G2, M1, M2
VCC_CKLK1 (2)	AA35	AF18	W24
VCC_CKLK2 (2)	W4	N11	Y9
VCC_CKLK3 (2)	T34	AC26	M24
VCC_CKLK4 (2)	R4	P10	P9
VCC_CKOUT1 (7)	U33	AF22	N24
VCC_CKOUT2 (7)	Y1	V7	AA9
GND	A1, A18, A35, AK18, AL18, AL30, AL5, AL6, AM18, AM2, AM3, AM31, AM32, AM33, AM34, AM4, AN1, AN18, AN2, AN3, AN34, AN35, AP1, AP18, AP2, AP34, AP35, AR1, AR18, AR35, B1, B18, B2, B34, B35, C18, C2, C3, C33, C34, C35, D18, D2, D3, D17, D32, D33, D34, D4, E18, E30, E31, E32, E33, E5, E6, F18, V1, V2, V3, V30, V31, V32, V33, V34, V4, V5, V6	A2, A8, A14, A19, A25, B1, B2, B6, B21, B25, B26, C3,C13, C24, D4, D23, H8, H19, J9, J18, K10, K17, L11, L13, L16, M12, M15, N1, N4, N13, N14, N26, P1, P2, P3, P13, P14, P23, P26 R12, R15, T11, T16, U10, U17, V9, V18, W8, W19, AC4, AC23, AD3, AD13, AD24, AE1, AE2, AE6, AE21, AE25, AE26, AF2, AF8, AF14, AF19, AF25, AF15	B2, B3, C2, C3, F3, F4, G3, G4, L3, L4, M3, M4, T1, T2, T3, AA3, AA4, AB3, AB4, AF3, AF4, AG3, AG4, AK2, AK3, AL2, AL3, AJ6, AJ7, AK6, AK7, AJ11, AJ12, AK11, AK12, AL16, AM16, AJ21, AJ22, AK21, AK22, AJ26, AJ27, AK26, AK27, AK30, AK31, AL30, AL31, AG29, AG30, AF29, AF30, AB29, AB30, AA29, AA30, U30, U31, U32, M29, M30, L29, L30, G29, G30, F29, F30, C30, C31, B30, B31, C26, C27, D26, D27, C21, C22, D21, D22, A17, B17, C11, C12, D11, D12, C6, C7, D6, D7
GND_CKLK1 (2)	Y30	AE18	V24
GND_CKLK2 (2)	W2	P11	V9
GND_CKLK3 (2)	T33, V35	AC25, N25	P24, P23
GND_CKLK4 (2)	R3	R10	T9
GND_CKOUT1 (7)	U32	AE22	T24
GND_CKOUT2 (7)	Y2	V6	W9

Pin Name	652-Pin BGA	672-Pin FineLine BGA	1,020-Pin FineLine BGA
No Connect (N.C.)			AA12, AA13, AA14, AA15, AA16, AA17, AA18, AA19, AA20, AA21, AB10, AB11, AB12, AB13, AB14, AB15, AB16, AB17, AB18, AB19, AB20, AB21, AB22, AB23, AB24, AB25, AB8, AB9, AC10, AC11, AC12, AC13, AC14, AC15, AC16, AC17, AC18, AC19, AC20, AC21, AC22, AC23, AC24, AC25, AC8, AC9, AD10, AD11, AD12, AD13, AD14, AD15, AD16, AD17, AD18, AD19, AD20, AD21, AD22, AD23, AD24, AD25, AD8, AD9, AE14,AE15, AE16, AE17, AE18, AE19, H11, H12, H13, H14, H15, H16, H17, H18, H19, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J20, J21, J22, J23, J24, J25, J9, K10, K11, K12, K13, K14, K15, K16, K17, K18, K19, K20, K21, K22, K23, K24, K25, K9, L10, L11, L12, L13, L14, L15, L16, L17, L18, L19, L20, L21, L22, L23, L24, L25, L9, M12, M13, M14, M15, M16, M17, M18, M19, M20, M21, N12, N13, N14, N15, N16, N17, N18, N19, N20, N21, P12, P13, P14, P15, P16, P17, P18, P19, P20, P21, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, T12, T13, T14, T15, T16, T17, T18, T19, T20, T21, U12, U13, U14, U15, U16, U17, U18, U19, U20, U21, V12, V13, V14, V15, V16, V17, V18, V19, V20, V21, W12, W13, W14, W15, W16, W17, W18, W19, W20, W21, Y12, Y13, Y14, Y15, Y16, Y17, Y18, Y19, Y20, Y21
Total User I/O Pins (11)	488	508	588

Notes:

(1) This pin can be used as a user I/O pin after configuration.

(2) This pin is the power or ground for the ClockLock and ClockBoost circuitry. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device. VCC_CKLK has the same voltage specifications as the VCCINT and should be connected to a 1.8-V power supply. If the ClockLock or ClockBoost circuitry is not used, this power or ground pin should be connected to VCCINT or GNDINT, respectively.

(3) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.

(4) This pin is the complementary signal for the LVDS pair on dedicated inputs and outputs that can be configured for the LVDS standard. If not used for the LVDS pair, these pins are regular I/O pins. Pins with the "n" suffix carry the negative signal for the LVDS channel. Pins with a "p" suffix carry the positive signal for the LVDS channel.

(5) This pin is a dedicated pin; it is not available as a user I/O pin.

(6) This pin is tri-stated in user mode.

(7) This pin is the power or ground for the external output of a PLL. These pins should be set to the VCCIO level/standard desired for the external clock ouput. To ensure noise resistance, the power and ground supply to the PLL external output should be isolated from the power and ground to the rest of the VCCIO and GNDIO pins. If the PLL or external output is not used, this power or ground pin should be connected to VCCIO or GNDIO, respectively.

(8) The CLKLK_OUT pin is powered by the VCC_CKOUT and GND_CKOUT pins.

(9) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry is locked to the incoming clock and generates an internal clock, LOCK is driven high. LOCK remains high if a periodic clock stops clocking. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.

(10) This pin is the active high enable pin for all of the PLL circuits in the device. When de-asserted, all PLLs are reset to their default, unlocked state and will stop clocking. Once re-asserted, the PLLs will lock again and start clocking. If this pin function is not needed, the pin should be connected to VCCINT.

(11) The user I/O pin count includes dedicated inputs and dedicated clock inputs. It does not include the dedicated clock feedback and output pins.